**TIE-UP**







**National Institute of Electronics and Information Technology   
(J&K)**

ISO 9001:2008 certified organization

**Department of Electronics & Information Technology (DeitY), Ministry of Communications and Information Technology, Govt. of India.**

**Contact us:**

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**National Institute of Electronics & Information Technology** (NIELIT),(erstwhile  DOEACC) was set up to carry out HRD-IT and related activities in the area of Information, Electronics & Communications Technology (IECT). NIELIT is engaged both in Formal & Non-Formal Education in the area of IECT besides development of industry oriented quality education and training programmes in the state-of-the-art areas. NIELIT has endeavoured to establish standards to be the country’s premier institution for Examination and Certification in the field of IECT. It is also one of the National Examination Body, which accredits institutes/organizations for conducting courses in IT in the non-formal sector.

NIELIT has thirty one (31) offices located, with a strong network of over 800 accredited institutes and over 6000 facilitation centres.

**About NIELIT Srinagar/Jammu**

* NIELIT J&K is functioning from Srinagar, Jammu & Leh.
* **Srinagar Centre is located in the SIDCO Electronics Complex, Rangreth on a 7.5 acres Campus with a built-up area of 33,000 sq.ft.**
* The Jammu Centre is located on the New Campus of the University of Jammu with a built-up area of 22,000 sqft.
* Sub-Centre Leh is located at Skalzangling, Airport Road, Leh.
* **Long Term Courses:** 
  + MCA in affiliation with University of Kashmir.
  + PGDCA in affiliation with University of Jammu.
  + Software/Hardware courses like ‘O’, ‘A’ & ‘B’ level.
* **Short Term Courses in:**
* **Computer Networking**
* CCNA,CCNP
* MCSA(Windows Server 2012)
* Linux Networking
* Integrated Networking Industrial Program.
* WSN (Wireless Sensor Networks)
* **Ethical Hacking and Cyber Forensics**
* Information Security, Ethical Hacking and Cyber Forensics
* **Programming courses**
* Android Programming
* .Net Technologies
* Programming in Java
* Embedded Systems Programming
* MATLAB
* Programming in C/C++
* **Open Source Technologies**
* PHP and MySQL
* Python
* **Database**
* Oracle SQL Dev,Oracle PL/SQL Dev,Oracle App Dev
* **Computer Aided Design**
* VLSI Designing
* AutoCAD
* **Basic Literacy Programs**
* DOEACC “CCC” Course
* Basic Computer Applications.
* **Others**
* Repair of Mobile Phones.
* PC Assembling and Testing
* Web Design
* Diploma in operation and Maintenance of Bio Med equ.

**Industrial Training**

**In**

**Computer Aided Design**

**(VLSI Designing )**

* CMOS Circuit design
* Transistor Sizing
* CMOS Processing steps
* Current trends

**Advanced Digital Design Using Altera**

* Introduction
* Arithmetic Circuits
* Data Processing Circuits
* Universal Logic Elements
* Combinational Circuits
* Sequential Circuits
* Latches, Registers, Counters
* PLDs & PLAs

[**VHDL-RTL**](http://www.roseindia.net/java/string-examples/) **Coding**

* Introduction to VHDL
* Data types
* Operators
* Assignments
* Code Coverage
* Mini Project based on the above knowledge

[**VHDL**](http://www.roseindia.net/java/exceptions/) **Synthesis**

* Hierarchical Design
* Combinational Circuit Design
* Sequential Design
* Defining and Throwing Exceptions
* FSM
* Design Synthesis

**Objective:** This comprehensive course is a thorough introduction to the VHDL language. The emphasis is on writing solid synthesizable code and enough simulation code to write a viable test bench. Structural, register transfer level (RTL), and behavioural coding styles are covered. This class addresses targeting ALTERA devices specifically and CPLD devices in general. The information gained can be applied to any digital design by using a top-down synthesis design approach. This course combines insightful lectures with practical lab exercises to reinforce key concepts.

**Eligibility:** MCA, BE/B.Tech, BCA and A/B Level students (Undergoing/Completed)

**Training Methodology**:

* Classroom Lectures
* PPT Presentations
* Hands on practice in well equipped labs

**VLSI Designing** (*Duration: 6weeks @2 hrs daily)*

**Introduction VLSI Design**

* VLSI Design flow
* FPGA Vs CPSL Vs ASIC
* RTL Design methodologies
* [EDA Tools](http://www.roseindia.net/java/beginners/sdk-directory-structure.shtml)
* Evolution of Integrated circuits

**CMOS Fundamentals**

* Non Ideal Characteristics
* BJT Vs FET
* Input Wrapper Class
* Fields and Methods
* Encapsulation
* Access Control
* Inheritance
* Polymorphism

**Android Activities and UI Design**

* Understanding Intent
* Activity Lifecycle and Manifest