C0-R4.B4 : COMPUTER SYSTEM ARCHITECTURE

NOTE :

- 1. Answer question 1 and any FOUR questions from 2 to 7.
- 2. Parts of the same question should be answered together and in the same sequence.

Total Time : 3 Hours

Total Marks : 100

- **1.** (a) What is tri-state buffer ? Draw a bus line using three state-buffers for four register A, B, C and D having 4 bits each.
 - (b) Represent the following conditional statement by two register transfer statement with control functions. If (P=1) then (R1←R2) else if (Q=1) then (R1←R3). Also draw the hardware to transfer data from register R1 to register R2 when P=1
 - (c) Using 8-bit 2's complement representation of negative numbers, perform the following computation: $(-35)_{10}+(-11)_{10}$
 - (d) What is Priority Interrupt? Explain Daisy-Chaining Priority Interrupt.
 - (e) Explain instruction cycle in CPU with a four-segment pipeline using flow diagram.
 - (f) Explain the following terms (any two)
 - (i) Locality of reference
 - (ii) Subroutines
 - (iii) Associative memory
 - (iv) Serial communication
 - (g) What is strobe and handshaking in asynchronous data transfer ?

(7x4)

- (a) Explain three different types of shift Micro operations. Apply those microoperation with an initial value of R=11011100. Determine the value of R after Logical Shift Left, followed by Circular Shift Right, followed by Logical Shift Right and Circular Shift Left.
 - (b) Draw the timing diagram assuming that SC is cleared to 0 at the time T3 if control signal C7 is active i.e. C7T3 : SC→0
 (C7 is activated with the positive clock transition associated with T1.)
 - (c) Explain interrupt cycle with the help of flowchart.

(6+4+8)

- 3. (a) Explain subtraction of unsigned binary numbers using 2's complement method.
 - (b) Explain the following instructions with help of some example
 - (i) Three-Address Instructions
 - (ii) Two-Address Instructions
 - (iii) One-Address Instructions
 - (iv) Zero-Address Instructions
 - (c) Explain various types of Addressing modes used to design general purpose computer.

(4+6+8)

- **4.** (a) Explain different types of hazards and dependencies in pipeline processors.
 - (b) The nonpipeline system takes 50ns to process a task. The same task can be processed in a six- segment pipeline with clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100ns task. What is the maximum speedup that can be achieved ?
 - (c) Write a program in assembly language to Input and Output one character in reference of Input-Output Programming.

(6+6+6)

- 5. (a) Explain these mode of transfer in brief :
 - (i) Programmed I/O
 - (ii) Interrupt-initiated I/O
 - (b) What is Direct Memory Access (DMA)? Explain block diagram of DMA controller and its working principles.
 - (c) What is Input-Output Processor (IOP) ? Explain sequence of operations carried out between CPU-IOP communications.

(6+6+6)

- 6. (a) A computer system uses a memory unit with 256k words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: An indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.
 - (i) How many bits are there in operation code, the register code part and address part ?
 - (ii) Draw the instruction word format and indicate the number of bits in each part.
 - (iii) How many bits are there in the data and address inputs of the memory ?
 - (b) Explain the following terms with reference of cache memory :
 - (i) Direct mapping
 - (ii) Associative mapping
 - (iii) Set-associative mapping
 - (c) Explain the concept of Virtual Memory.
- 7. (a) (i) Solve $(-9)_{10}^{*}(-13)_{10}$ using Booth's Multiplication algorithm.
 - (ii) Solve division using Division Algorithm taking Divisor B=10001 & Dividend A=0111000000
 - (b) Explain the following architectures and give example of each.
 - (i) SISD
 - (ii) SIMD
 - (iii) MISD
 - (iv) MIMD

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(7+6+5)

(12+6)