C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Show a block schematic of a hardware construction for implementing the following control function:
P: R2 ← R1 where R1 and R2 both are n bit registers.

b) Each line of an assembly language program is arranged in certain number of fields. Specify these fields and show the information provided by each field.

c) Explain the difference between hardwired control and micro-programmed control. Is it possible to have a hardwired control associated with a control memory?

d) Explain Register Indirect mode of addressing instruction. What is the advantage of defining this mode of addressing?

e) Explain in brief, superscalar processor architecture.

f) What major differences exist between the CPU and peripherals?

g) Why is the cache memory employed in computer systems?

(7x4)

2.

a) Design a 4 bit arithmetic circuit using a 4 bit adder and 4 multiplexers which generates the eight arithmetic operations shown in the following table:

Select			Input	Output	Microoperation
S_1	S_0	C_{in}	Y	$D = A + Y + C_{in}$	
0	0	0	B	D = A + B	Add
0	0	1	B	D = A + B + 1	Add with carry
0	1	0	$\overline{B}$	D = A + $\overline{B}$	Subtract with borrow
0	1	1	$\overline{B}$	D = A + $\overline{B}$ + 1	Subtract
1	0	0	0	D = A	Transfer A
1	0	1	0	D = A + 1	Increment A
1	1	0	1	D = A – 1	Decrement A
1	1	1	1	D = A	Transfer A

b) Although there are 16 logic microoperations, most computers use only four, which are listed in the following function table:

S_1	S_0	Output	Operation
0	0	$E = A \cdot B$	AND
0	1	E = A + B	OR
1	0	$E = A \oplus B$	XOR
1	1	E = $\overline{A}$	Complement

Using 4 gates (as required) and a multiplexer, draw a logic diagram of one stage of a circuit.

c) In the basic computer, the OR operation is not available as a machine instruction. Write a program to perform the OR operation using AND, CMA, STA and LDA instructions.

(8+4+6)

3.

a) The following transfer statements specify a memory operation. Explain the memory operations in each case.
   i) R2← M [AR]
   ii) M [AR] ← R3
   iii) R5 ← M [R5]

b) Define stack and stack pointer as applied to a microprocessor. What do you understand by the PUSH and POP instructions for insertion and deletion of items?

c) Write programs to evaluate the arithmetic statement:
   X = (A + B) * (C + D) using
   i) 3 – address instructions
   ii) 2 – address instructions
   iii) 1 – address instructions
   iv) Zero – address instructions

(6+4+8)

4.

a) Discuss the essential goals of CISC and RISC architecture? Describe the major characteristics of CISC and RISC processor.

b) Suppose that we want to perform the combined multiply and add operations with a stream of numbers as follows:
   $A_i * B_i + C_i$ for i = 1,2,3, …..7
   Implement each suboperation in a segment within a pipeline. Draw a block diagram and show the content of registers in pipeline for each clock cycle.

(8+10)

5.

a) Design an array multiplier circuit that multiplies a binary number of four bits with a number of three bits to produce a product of seven bits using two 4 bit adders and required number of AND gates.

b) Draw a block diagram for data transfer from I/O device to CPU through an interface.

c) Explain the terms: bus request and bus grant as applied to direct memory access (DMA). What is the purpose of cycle stealing?

(8+4+6)

6.

a) Enumerate the most striking difference between an I/O processor and a data communication processor, for communicating with the I/O devices.

b) Explain the concept of Branch delay.

c) Define a term “Virtual memory” as applied in large computer systems.

d) Describe the purpose of basic components of a memory management system as applied to multiprogramming environment.

(4+4+4+6)

7.

a) Differentiate between tightly coupled multiprocessor and loosely coupled multiprocessor. Which is more efficient in terms of interaction between tasks?

b) Draw a block schematic for implementing a dual system bus structure for multiprocessors showing CPU, IOP, local memory and system bus controller.

c) What are the advantages and disadvantages of the SISD and MISD architecture?

d) Explain 4 major groups on which Flynn’s classification is divided? What are the attributes on which, this classification depends?

(4+4+4+6)