B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

अवधि: 03 घंटे **अधिकतम अंक: 100**

DURATION: 03 Hours **MAXIMUM MARKS: 100**

ओएमआर शीट सं.: **OMR Sheet No.:**						

रोल नं.: **Roll No.:** | | | | | | |

उत्तर-पुस्तिका सं.: **Answer Sheet No.:** | | | | | | |

परीक्षार्थी का नाम: **परीक्षार्थी के हस्ताक्षर**:

Name of Candidate: _____; Signature of candidate: _____

परीक्षार्थियों के लिए निर्देश:	**Instructions for Candidate:**
कृपया प्रश्न-पुस्तिका**,** ओएमआर शीट एवं उत्तर-पुस्तिका में दिये गए निर्देशों को ध्यान पूर्वक पढ़ें।	Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.
प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी केवल अंग्रेजी भाषा में ही उत्तर दे सकता है।	Question Paper is in English language. Candidate can answer in English language only.
इस मॉड्यूल/पेपर के **दो भाग** है। **भाग एक** में चार प्रश्न और **भाग दो** में पाँच प्रश्न है।	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions**.**
भाग एक "वैकल्पिक" प्रकार का है जिसके कुल अंक 40 है तथा **भाग दो**, "व्यक्तिपरक" प्रकार है और इसके कुल अंक 60 है।	**PART ONE** is Objective type and carries 40 Marks. **PART TWO** is subjective type and carries 60 Marks.
भाग एक के उत्तर, इस प्रश्न-पत्र के साथ दी गई **ओएमआर उत्तर-पुस्तिका** पर**,** उसमें दिये गए अनुदेशों के अनुसार ही दिये जाने है। **भाग दो** की उत्तर-पुस्तिका में **भाग एक** के उत्तर **नहीं** दिये जाने चाहिए।	**PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book for **PART TWO**.
भाग एक के लिए अधिकतम समय सीमा **एक घण्टा** निर्धारित की गई है। **भाग दो** की उत्तर-पुस्तिका, **भाग एक** की उत्तर-पुस्तिका जमा कराने के पश्चात दी जाएगी। तथापि, निर्धारित एक घंटे से पहले **भाग एक** पूरा करने वाले परीक्षार्थी **भाग एक** की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरंत बाद, **भाग दो** की उत्तर-पुस्तिका ले सकते हैं।	Maximum time allotted for **PART ONE** is **ONE HOUR.** Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE.**
परीक्षार्थी, उपस्थिति-पत्रिका पर हस्ताक्षर किए बिना एवं अपनी उत्तर-पुस्तिका, निरीक्षक को सौंपे बिना, परीक्षा हाल नहीं छोड़ सकता हैं। ऐसा नही करने पर, परीक्षार्थी को इस मॉड्यूल/पेपर में अयोग्य घोषित कर दिया जाएगा।	**Candidate cannot leave the examination hall/room without signing on the attendance sheet and handing over his Answer sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.**
प्रश्न-पुस्तिका को खोलने के निर्देश मिलने के पश्चात एवं उत्तर देने से पहले उम्मीदवार यह जाँच कर यह सुनिश्चित कर ले कि प्रश्न-पुस्तिका प्रत्येक दृष्टि से संपूर्ण है।	After receiving the instruction to open the booklet and before answering the questions, the candidate should ensure that the Question booklet is complete in all respect.

जब तक आपसे कहा न जाए तब तक प्रश्न-पुस्तिका न खोलें।

DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 A combinational circuit that converts binary information from *n* inputs line to a maximum of unique output lines is known as
A) Decoder B) Encoder
C) Multiplexer D) Full Adder

1.2 Conversion of hexadecimal number AFI to its equivalent binary number is
A) 101111100001 B) 110111010001
C) 101011110001 C) 101111000001

1.3 A full adder is simply a connection of two half-adder joined by
A) AND gate B) OR gate
C) NAND gate D) NOR gate

1.4 The DMA transfer technique where transfer of one word data at a time is called
A) Memory Stealing B) Cycle Stealing
C) Memory Interleaving D) None of the above

1.5 What is the representation of -127 in 2's complement form using 8-bits?
A) 00000000 B) 11111111
C) 10000000 D) 10000001

1.6 Simplified form for Boolean algebraic expression F=XYZ' + XYZ + XY' (where ' represents complement of the variable) is
A) XY B) X
C) X' D) Y'

1.7 Consider DR ← M [AR], Identify the operation
A) Opcode Fetch B) Memory Write
C) Memory Read D) None of the above

1.8 Which of the following addressing modes specifies a register which contains the memory address of the operand?
A) Register Addressing Mode
B) Register Indirect Addressing Mode
C) Indexed Addressing Mode
D) Immediate Addressing Mode

1.9 What is the size of address bus in 8086 microprocessor?
A) 8 - bits B) 16 - bits
C) 20 - bits D) 24 - bits

1.10 In case of Zero-address Instruction Method the operands are stored in
A) Registers B) Accumulators
C) Push Down Stack D) Cache

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 It is very easy to make any modification in hardwired control unit.

2.2 Flip-flop is a sequential circuit.

2.3 Output of Ex-OR gate is high if input contains even number of one.

2.4 While executing instructions, the address of the next instruction to be fetched from the memory address is stored in memory address register.

2.5 STA instruction uses direct addressing mode.

2.6 A table that lists the required inputs for a given change of state is known as excitation table.

2.7 NOR gate is considered as a universal gate.

2.8 Cache memory is a memory which will store least frequently used data.

2.9 The booth algorithm generates a 2 n-bit product and treats both positive and negative 2's-complement uniformly.

2.10 RAM is a non-volatile memory.

ROUGH WORK SPACE:

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

X		Y	
3.1	2^n input and n output	**A.**	Program Counter
3.2	LDA instruction	**B.**	Flip-Flop
3.3	A computer with hardwired control unit	**C.**	Encoder
3.4	Shift register is a cascading of	**D.**	Associate Memory
3.5	Content Addressable Memory	**E.**	93
3.6	Principle of locality	**F.**	2 GB
3.7	2048 Megabtyes	**G.**	RISC
3.8	Pen drive is an example of	**H.**	Cache Memory
3.9	Register which will store of next instruction is	**I.**	Memory Read Operation
3.10	BCD of 10010011	**J.**	1 GB
		K.	Flash Memory
		L.	91
		M.	Stack Pointer

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Choose the most appropriate option, enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	Parallelism	**B.**	Left	**C.**	Programmed
D.	Booth	**E.**	6	**F.**	Throughput
G.	Status	**H.**	RS	**I.**	Implied
J.	150	**K.**	144	**L.**	Counter
M.	Encoder				

4.1 For multiplying a binary fixed point number by 32, shift _____ by five bits.

4.2 Pipelined architecture is used to implement _____.

4.3 Instruction without any operand is known as _____ addressing mode instruction.

4.4 Memory mapped I/O is better than _____ I/O.

4.5 in 8086 processor the size of prefetch queue is _____ bytes.

4.6 A JK flip-flop is refinement of _____ flip-flop.

4.7 A decimal 100 is an equivalent of octal _____.

4.8 A register which goes through a predetermined sequence of states upon application of input pulse is called _____.

4.9 _____ algorithms include repeated addition of two predetermined values to a product and then perform rightward arithmetic shift on product.

4.10 The register used to store the flats is known as _____ register.

ROUGH WORK SPACE:

PART TWO
(Answer any FOUR questions)

5.

a) Perform the operations 1234 – 1000 of two unsigned number using 10's complement.
b) Design a 4-bit combinational circuit decrementer using four full adder.
c) Define instruction cycle. Explain instruction cycle in detail with flowchart.

(3+4+8)

6.

a) Explain memory organization in brief.
b) What is addressing mode? Explain direct and indirect addressing mode using an example.
c) Draw the logic diagram of D Flip-Flop and give its truth table and characteristic table.
d) Differentiate software interrupt and hardware interrupt.

(5+3+5+2)

7.

a) Write a short note on asynchronous data transfer.
b) Write a short note on Micro Programmed Control Unit.
c) Explain direct mapping scheme of cache memory. List down the disadvantage of direct mapping scheme of cache memory. Compare direct mapping with set associative memory.

(4+4+7)

8.

a) Explain the working of DMA (Direct Memory Access) transfer mechanism.
b) How many address lines and input, output data lines are needed for a memory unit of 1 GB x 32 (where 1GB is the number of words and word length is 32 bits)?
c) Write a short note on arithmetic pipelining in details.

(5+3+7)

9.

a) Using booth algorithm of signed 2's complement multiplication perform the multiplication of (-9) X (-13).
b) Write an assembly language program to calculate the factorial of a given number.
c) What is multiplexer? Draw and explain 4 to 1 multiplexer with truth table and function table.

(5+5+5)

*****

ROUGH WORK SPACE:

ROUGH WORK SPACE: