C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Draw the diagram of a 4-bit combinational circuit incrementer using half-address and explain.

b) The following transfer statements specify a memory. Explain the memory operation in each case.

i) R2 ← M[AR]

ii) M[AR] ← R3

iii) R5 ← M[R5]

c) Explain the difference hardwired and microprogrammed control unit.

d) What are CISC and RISC architecture? How do they differ from each other?

e) Write the Assembly language program to subtract two numbers.

f) Explain how the instruction cycle in the CPU can be processed with a four-segment pipeline.

g) How DMA improves I/O operation efficiency?

(7x4)

2.

a) Calculate how many clock cycles will take execution of this segment on the simple pipeline without forwarding or bypassing when result of the branch instruction (new PC content) is available after WB stage. Show timing of one loop cycle in below figure:

Instruction	**Clock Cycle Number** **1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17**
L W R1, 0 (R4)	
L W R2, 400 (R4)	
ADD1 R3, R1, R2	
SW R3, 0 (R4)	
SUB R4, R4, #4	
BNEZ R4, L1	

b) What is a microinstruction? Write a micro instruction code format and explain all the fields in it.

(10+8)

3.

a) List and briefly define four types of computer system organization of Flynn's classification.

b) Explain with an example, how effective address is calculated in different types of addressing modes.

c) What is direct memory access (DMA)? Why are the read and write control lines in a DMA controller bi directional?

(6+6+6)

4.

a) Draw and Explain Common Bus System. Write the step to load value from the memory address is stored in Program Counter register.

b) Use the booth algorithm to multiply 14(multiplicand) by -5(multiplier), where each number is represented using 5-bit singed nos.

c) Perform addition and subtraction using singed 2's complement system.

1) $(-29)_{10} + (-49)_{10}$

2) $(1001)_2 - (101000)_2$

(8+6+4)

5.

a) Design and explain 4-bit combination circuit decrementer using four full-adder circuits.

b) What are the various floating point representation in IEEE754 standard.

c) Is it possible to design an expanding opcode to allow the following to be encoded in a 12-bit instruction? Assume a register operand requires 3 bits and this instruction set does not allow memory addresses to be directly used in an instruction

(6+6+6)

6.

a) List common addressing techniques. Explain any three of them in detail.

b) What are the interrupts? Explain different types of interrupts.

(10+8)

7.

a) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.

b) What do you mean by micro-programmed control unit? Illustrate with proper diagram.

c) Write short notes on followings:

i) Associate Memory

ii) Program Status Word (PSW)

(6+6+6)