

CEDTI Complex, Dr. B.A.M. University campus Aurangabad, Maharashtra-431004 <u>http://www.nielit.gov.in/aurangabad/</u>



Online Certificate Course in VLSI Design

Course Duration - 28 Hours

Theory-1Hr. & Lab-1 Hr.

Course Description:

- > Hardware Modeling Overview.
- > VHDL & Verilog language concepts.
- > Test benches Writing.
- Coding for Synthesis.
- > FPGA Architecture Basic Components of FPGA (LUT, CLB, Switch Matrix, IOB).
- > FPGA Architecture of different families: Artix-7 FPGA and Basys-3 Board.
- FPGA Design Flow Xilinx Vivado tool, Reading Reports, SSN and Implementing IP cores, soft-core processor IP Design using MicroBlez.
- Optimal FPGA Design HDL Coding Techniques for FPGA, FPGA Design Techniques.
- > Synthesis Techniques, Implementation Options.

Eligibility:

Diploma/B.Sc./M.Sc./B.Tech./M.Tech. in Electronics/Electrical/Science stream/ Instrumentation (Completed or Pursuing).

Prerequisite:

Basic Knowledge of Analog & Digital circuits.

Fee & Important dates:

Last Date for Registration & Payment	Expected Date of Course Start	Course Fee
Last Friday of every odd month	First Monday of every even month	Rs. 1,200/- incl. GST & all other charges

Total - 2 Hrs. per Da

Mode of Course Delivery:

The course would be conducted in virtual classroom environment which will be completely online, Course content includes Online Theory & lab sessions, Live interactive doubt clearance sessions, Course material in text/pdf format, Links to external resources and blogs, Online Forums, Lab Assignments, Tests etc.

Certificate:

Certificate will be provided to the participants, based on minimum 75% attendance and on performance (minimum 50% marks) in the online test, conducted at the end of the course.

How to Apply:

- Read the course structure & course requirements carefully.
- > Visit the Registration portal and click on apply button.
- Create your login credentials, fill up all the required details, check preview and Submit the application form.
- Login with your credentials to verify the mobile number, amail:10 and then upload the documents, Lock the profile and Pay the Fees online, dsing ATM-Debit Card / Credit Card / Internet Banking / UPI etc.

Contact Person:

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Course Coordinator:

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Course Content

Theory Topics	Hours	Practical/Lab Assignments	Hours
Introduction to VHDL	1 Hrs	 → How to download and Install Vivado Software → Install web pack License on Vivado 	1 Hrsv
Introduction to Verilog	1 Hrs	→ How to create Project in Vivado with example	1 Hrs
 Detail modeling's of Verilog 1. Behavioral modeling 2. Data flow modeling 3. Gate level modeling 4. Switch level modeling 	4 Hrs	→ How to write Test bench waveform with example	1 Hrs
Introduction to ASIC and FPGA- FPGA design flow	1 Hrs	→ How to write constraint files in Vivado	2 Hrs
 Introduction To combinational Circuits and its various examples 	Hirs	Synthesis of combinational logic Examples	2 Hrs
 Introduction To Sequential Circuits and its various examples 	2 Hrs	 Synthesis of sequential logic Examples 	2 Hrs
Introduction To FSM Chouits and its various examples	1 Hrs	→ Synthesis of FSM Examples	1 Hrs
 Introduction To ASM Circuits and its various examples 	1 Hrs	→ How to use IP in Vivado	1 Hrs
Vehilog Function & Tasks	1 Hrs	 → Practice Examples → Examples Using Basys-3 Board 	2 Hrs
Mini Project (Real time project)	1 Hrs	→ Complete Mini Project	1 Hrs