Design of a Reconfigurable Hardware Platform for Medical Ultrasound Imaging and Research

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Abstract This paper discusses the creation and progress of a 128-channel digital reconfigurable hardware, which is used in medical ultrasound imaging systems and for research purposes. A novel digital hardware solution that incorporates a high-end field programmable gate array (FPGA) is proposed here alongside a high-speed FPGA mezzanine connector (FMC), PCIe 2.0 × 8, and Gigabit Ethernet links. Essential components such as clock, power tree, module for power management, logic for debugging etc. are integrated into the hardware design. This FPGA-based hardware solution enables the investigation of medical ultrasound signal processing solutions on an FPGA platform. This advanced technology can be linked to a 128-channel ultrasound transceiver and a computer to create a prototype for an ultrasonic imaging system. The hardware solution's FPGA-based nature offers flexibility in reconfiguring the hardware for medical ultra-sound imaging systems. Furthermore, this work provides a single board solution for implementing ultrasound systems using several channels.

Keywords Digital beamformer hardware · Reconfigurable hardware · FPGA · PCIe · Gigabit Ethernet · PMBus™

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P. Shivakumara et al. (eds.), *Proceedings of the NIELIT's International Conference on Communication, Electronics and Digital Technologies*, Lecture Notes in Networks and Systems 1522, https://doi.org/10.1007/978-981-96-9932-2_5

1 Introduction

Ultrasound imaging serves as a widely adopted diagnostic method, leveraging focused sound wave energy to generate detailed images of biological tissues within the human body [1]. This method utilizes a combination of crucial elements, such as the transmit module (Tx), receiver (Rx) module, control circuitry, displays, power supplies. Notably, the ultrasound system requires both high voltage (HV) and low voltage (LV) power sections to drive the transmitter and to support the receiver module, ensuring efficient operation across a wide range of ultrasound imaging tasks. Figure 1 illustrates the frontend and mid-end processing modules of an ultrasound imaging system. In this representation, a collection of transducers, each with n elements/channels, is used to detect the ultrasound echoes that bounce back from the tissue. In the analog front end (AFE), the analog radio frequency (RF) echoes are amplified by a low noise amplifier (LNA), and then further amplified or attenuated based on depth proportional gain using time gain compensation (TGC) [2]. Subsequently, the signals are converted into digital format using an analog-to-digital converter (ADC). The digitized rf signals experience delay, apodization, and summation within the beam-former unit [3]. The resulting beamformed signal that corresponds to n channels of rf echoes, then undergoes envelope detection, logarithmic compression, and scan conversion to generate a diagnostic ultrasound image [4].

Thanks to advances in technology, ultrasound screening systems have made significant advances, including real-time and high image-rate imaging, such as 3D/4D imaging. As shown in Fig. 1, the remaining components of the ultrasonic screen system are related to electronics technology, except for the ultrasonic converter channel (array). As a result, the breakthroughs of electronic equipment including Field Programmable Gate Array (FPGA) and ASIC development has played a central role in the activation of ultrasound images [5]. The development of FPGA technology has made it easier to integrate hardware which supports digital signal processing. FPGAs when combines protocols such as Ethernet, High-speed Serdes, and PCIe [6]. Furthermore, FPGA technology allows for hardware acceleration of ultrasonic interference-algorithms while reducing power consumption [2]. Despite technological advances, ultrasound scanners with both cart-based and portable scanners, can be easily user control by receiving hardware modules, especially for researchers. As a result, numerous open platforms have been developed for research purposes to provide access to extremely healthy signal chains. In the summary paper [7],

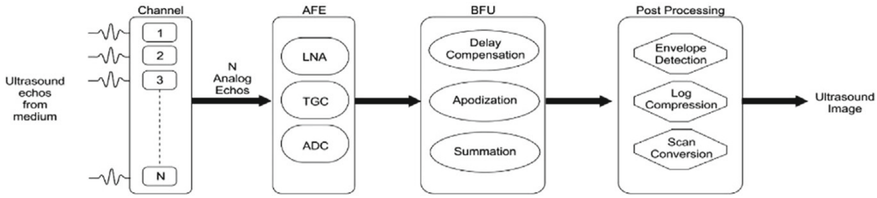

Fig. 1 Medical ultrasound imaging system-frontend and midend processing

existing ultrasound platforms have been evaluated for research. This focuses on hardware processing capabilities delivery throughput (IO) [8]. We had discussed about various ultrasonic system architectures in the article uses front-end and mid-end processing along with FPGA, which is connected to back-end processing via Personal Computer [2, 7, 9, 10]. These open ultrasound system architectures often rely on multiple boards to accommodate multi-channel systems, with researchers unable to access or configure the FPGA logic directly.

This paper presents a new single-board reconfigurable platform tailored for ultrasound receive signal processing applications. Our hardware platform, centered around FPGA technology, supports up to 128 channels and enables seamless interfacing with analog frontend modules and PCs via Gigabit Ethernet and PCIe interfaces, respectively. The paper is structured as follows: Sect. 2 reviews related works. Section 3 explores hardware design aspects, covering design considerations and implementation details. Fabrication and testing are thoroughly discussed in Sect. 4. Section 5 provides insightful discussions on related existing works. Finally, Sect. 6 presents conclusions drawn from the development work, summarizing contributions and suggesting potential future directions for the platform.

2 Related Works

The examination of many ultrasound imaging systems which are based on the field programmable arrays are covered in-detail in this section [11–14]. In the first design [11] that was shown, a complete functionality of the scanner which includes Transmit section, receive section, mid-end processing, back-end processing, and control functions are integrated onto one FPGA in a 16-channel portable device. A high-speed digital IO interface and FPGA-based timing control are the main features of the following architecture [8, 14]. The digitized ultrasonic raw sensor data which is high-speed digital is sent to a personal computer. The image processing will be completed after the transfer and the ultrasound image will be created. The timing controller makes it easier for the frontend modules to synchronize. In the third design, the prototype makes use of pre-existing evaluation boards, and the imaging system architecture integrates FPGA-based transmit and receive beamforming. Once more, scaled-down versions with 16/8 channels were used to showcase the systems [2].

The development of a ultrasound imaging beamformer which is 128 channel using FPGA is described in the article [12]. The beamformer must be built using 16-channel boards based on 8 FPGAs, which makes this system laborious. It streams beamformed ultrasonic data to a PC over a USB 2.0 interface, enabling the PC to handle picture creation and backend processing. This setup makes it easier to test and investigate novel imaging methods. Another ultrasonic imaging system, described in [14], helps in the creation and testing of new ultrasound research techniques by using hardware to feed raw RF data to a Personal computer via a high-speed interface, here we are using FPGA as hardware. Eight FPGA-based sixteen-channel frontend boards are used in a flexible multi-channel system described in [14] to create a 128-channel system. In [15–23], the significance of using FPGA in medical imaging is covered. Additionally, studies reported in [17, 19] demonstrate the use of adaptive beam-forming cores for ultrasonic imaging. It is essential to have FPGA-based reconfigurable processing hardware in order to evaluate equivalent algorithm implementations on FPGAs. The literature survey of relevant research emphasizes the need to investigate novel implementations of ultrasonic signal processing techniques using FPGA-based reconfigurable hardware. Additionally, a single-board solution that can perform the ultrasonic receive signal processing chain is required in order to design compact devices that may be used on carts or carried about. This study presents a single-board reconfigurable hardware solution with high-speed interfaces like PCIe and Gigabit Ethernet that can integrate up to 128 ultrasonic frontend channels. The full design of the FPGA-based reconfigurable hardware architecture is covered in detail in the next section.

3 Hardware Design

The developed ultrasound receive signal processing system architecture is depicted in Fig. 2. A single Kintex-7 FPGA, an interface for 128-channes ultrasound frontend hardware, and a number of other interfaces, including universal asynchronous receiver/transmitter (UART), QSPI Flash [2], byte peripheral interface (BPI) Flash, SD Card, JTAG, and peripheral component interconnect express (PCIe), are the main components of the hardware platform. This design offers a platform for implementing an ultrasound receive signal chain capable of handling up to 128 channels. The board incorporates non-volatile flash memory (QSPI Flash) for FPGA configuration and another (QSPI Flash) for storing delay values. Additionally, a BPI Flash is provided for storing FPGA configuration data. The receive beamforming can be achieved using the FPGA [3, 19, 20].

The JTAG/USB interface is included to facilitate connectivity between the board and PC, greatly aiding in troubleshooting processes. Additionally, a USB/UART interface is provided for simplified trouble shooting procedures. PCIe Gen 2 ($\times 8$) is utilized for transferring signal processed data to the CPU board for subsequent processing. Moreover, a Gigabit Ethernet Interface serves as a backup interface in case of PCIe failure.

The subsequent subsections delve into the various sub-blocks within the hardware platform.

3.1 FPGA

The Kintex-7 FPGAs represent Xilinx's pioneering venture into 28 nm technology [24]. These FPGAs offer a doubled price-performance ratio and halved power consumption compared to previous models. Designers often favor Kintex FPGAs for

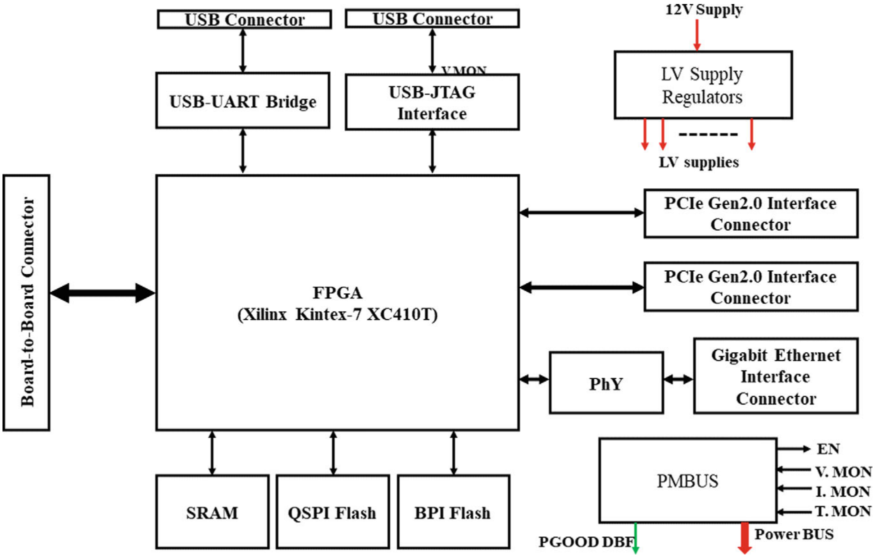

Fig. 2 Reconfigurable hardware platform

"high-end wireless communication" applications and in the field of medical ultrasound due to their capabilities. Because the cores can function at extremely low voltages of 1.0 or 0.9 V, less power is used and less cooling is needed. The XC7K410T FPGA model has been chosen for the Receiver Board. It has 63,550 slices, 406,720 logic cells, 28,620 Kb of Block RAM, 1,540 DSP48 Slices, 500 Single Ended I/O, and 240 Differential I/O pairs. Table 1 provides a concise overview of the resources available within the "Xilinx Kintex-7 XC7K410T FPGA".

The XC7K410T features dedicated hard IP support for eight channels of PCIe (Gen1/Gen2) and supports 16 "high-speed serial transceivers of GTX" grade, capable of handling up to 12.5 Gbps per channel. It includes a total of ten I/O blocks, with three high-performance (HP) banks and seven high range (HR) banks. Each bank

Table 1 Resources available in Xilinx Kintex-7 XC7K410T FPGA

Recourses	Details	Count
Logic	Slice	63,550
	Logic cells	406,720
	CLB flip-flops	508,400
Memory	Distributed RAM (Kb)	5,663
	Block RAM (Kb)	795
Clock	Clock management tiles	10
I/O	Single ended	500
	Differential	240

comprises 50 pins, with 48 supporting differential signaling. HR banks can operate from 1.2 to 3.3 V, while HP banks can operate from 1.2 to 1.8 V. A DSP48 slice consists of a pre-adder, a 25*18 bit multiplier, a 48-bit accumulator, an arithmetic unit, a logic unit, and a 48-bit pattern detector. Each LUT comprises two 32-bit ROM blocks, and each slice comprises four LUTs and eight flip-flop units, along with multiplexers and arithmetic carry logic. Two such slices combine to form one configurable logic block (CLB).

3.2 "Power Management and Debug Bus" (PMBus™)

The TI® UCD90320 device functions as the PMBus™ module in the suggested design. Up to 32 power rails are supported by this module for management and sequencing [2]. It incorporates 24 ADCs for supply current, voltage, and temperature monitoring in addition to power sequencing and control. For the FPGA to operate properly in the intended architecture, precise power-on and power-off sequencing is required. Through the power enabling pins, the PMBus™ UCD90320 can be set up to control the sequencing of devices' power-on and power-off operations. FPGA power-on and power-off sequencing, for example, is essential. The core voltage must be activated before turning on any IO supplies to prevent current from leaking into the core and potentially harming the device. Low voltage (LV) supplies are required for parts like the FPGA, UCD90320, clock tree section, etc. by the hardware architecture [2]. The power tree design incorporates low drop out (LDO) regulators and DC to DC converters to address this requirement. Either an LDO alone or a DC to DC converter followed by an LDO is used in circuits that are susceptible to noise. For dependable circuit functioning, monitoring rail voltages, currents, fault states, etc., is essential in addition to power sequencing. Temperature, voltage, and current tolerance thresholds can be set on the device. Any power rail that deviates from these tolerances can be turned off, and the PMBus™ controller interface can be used to retrieve fault information.

3.3 Clock Circuitry

Figure 3 illustrates the clock network of the hardware platform. The FPGA system clock is generated from the SiT910 chip in low voltage differential signalling (LVDS) format, operating at 200 MHz frequency. The user clock is derived from the Si570 chip, which can be programmed via I2C interface by the FPGA itself to produce frequencies ranging from 10 to 810 MHz in LVDS format. Additionally, an external master configuration clock of 66 MHz in LVCMOS format is supplied to the FPGA from the SIT8103. The FPGA can choose either the internal clock or this external clock for configuration purposes. Furthermore, a LVDS Clock of 125 MHz is supplied to the FPGA from the 84402A XTAL to LVDS clock generator, which generates the

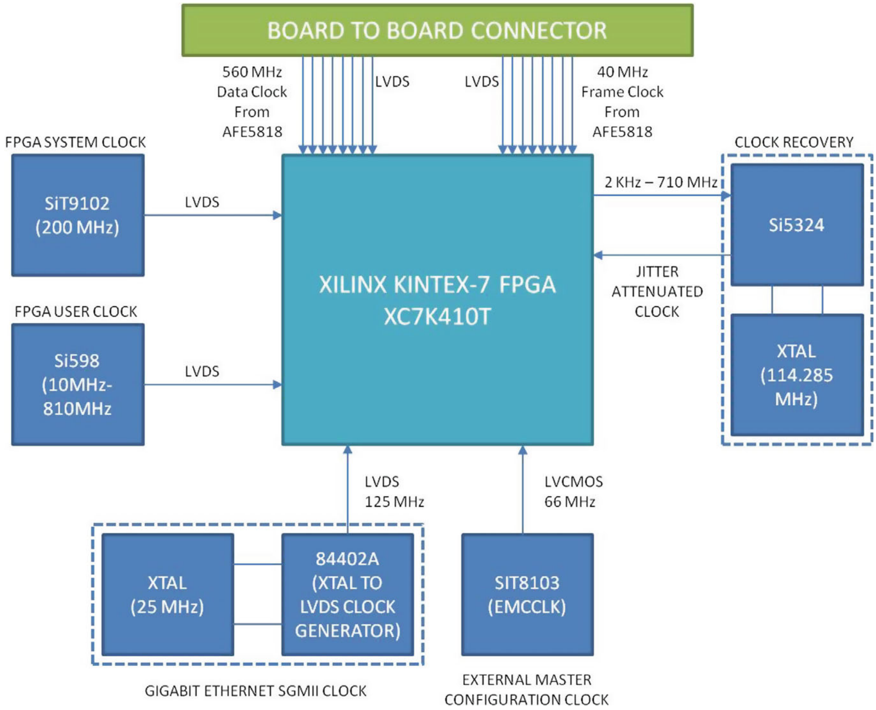

Fig. 3 Clock circuitry

125 MHz clock from a 25 MHz crystal oscillator. This clock is intended for the SGMII interface of the Gigabit Ethernet PHY chip M88E1111-XX-BAB1C000.

In the design, a clock recovery circuit utilizing the Si5324 (clock multiplier and jitter cleaner) has been incorporated. The FPGA is tasked with supplying an input clock ranging from 2 kHz to 710 MHz to the Si5324. The Si5324, in turn, generates a jitter-attenuated LVDS clock and supplies it to the FPGA. The frequency of this clock can be programmed to the Si5324 using the I2C interface. Additionally, the FPGA is responsible for handling eight data clocks (each operating at 560 MHz LVDS) and eight Frame Clocks (each at 40 MHz LVDS) from the eight AFE chips in the transceiver board. Each AFE chip supplies 16 channels of data through 16 LVDS lines.

3.4 *Flash Memory*

In order to boot the bit file and store the receiving beamformer delay configurations, a 256 Mb serial NOR Flash memory has been selected to link with the FPGA [2]. The first high-performance multiple input/output serial Flash memory produced with 65 nm NOR technology is this device. It has a high-speed SPI-compatible bus interface, execute-in-place (XIP) functionality, and sophisticated write protection features. By increasing the transmission capacity for READ and PROGRAM operations, the novel dual and quad input/output instructions essentially double or quadruple the speed.

3.5 Interfaces

The hardware platform requires interfacing with ultrasound transceiver hardware and a PC. Signal-conditioned and digitized analog echo signals must be transferred from the receive hardware, where receive signal processing, including beamforming, is performed. The processed receive signal data can then be transferred to a PC for post-processing and display. Gigabit Ethernet, PCIe, and board-to-board interfaces are used to manage IO data flow. The most common protocols used in control interfaces are SPI, I2C, and UART. An overview of the interfaces used in the design is given in Table 2, along with descriptions of each.

3.6 AC and DC Analysis

Pin-level interconnect compatibility must be guaranteed by AC and DC analysis after the components have been chosen and the architecture design is finished [2]. By figuring out the total drive capacitance required, AC analysis determines the necessary drive strength. This means that all other drive input capacitances must

Table 2 XXX

Sl. no	Protocol	Details
1	SPI flash	The link between Flash and FPGA. Allows for up to four lines (QSPI). Both flash read/write and FPGA boot from flash [2]
2	SPI	Serial interface to configure other controller ICs
3	I^2C	The FPGA user clock interface with the programmable oscillator [2]
4	UART	FPGA and PC interface. Using the CP2103, the serial port was accessed through the USB connector, here we use USB to UART converter
5	JTAG	.bit file uploading and debugging [2]
6	PCIe/Gigabit ethernet	High speed interfaces to interface with PC
7	"Board to Board Connector"	Signals are conditioned and digital LVDS are transferred from transceiver hardware

be less than the load capacitance. Conversely, DC analysis examines pin voltage compatibility while taking both high and low logic levels into account. Appropriate buffers can be used to remedy any drive strength issues, and level translators can be used to address voltage compatibility issues. These steps guarantee the system's compatibility and smooth operation.

4 Fabrication and Testing

After completing the schematic capture and component placement, the next steps involve analyzing the signal integrity, power consumption, and thermal performance of the created PCB. After this procedure, the manufactured and component-populated Ultrasound reconfigurable receiver hardware is shown in Fig. 4. A PC-based automated test program has been created to verify the interfaces. A serial port-based test control technique is used, and the FPGA and PC are interfaced via the UART [2]. The created test GUI makes it possible to efficiently test a variety of interfaces and signal chains.

The receiver signal chain has been validated, and the created ultrasonic receive hardware has been successfully integrated with the "ultrasound system prototype". The created system prototype is depicted in Fig. 5. This configuration uses a "board-to-board connector" to feed the digitalized and "signal-conditioned" analog radio

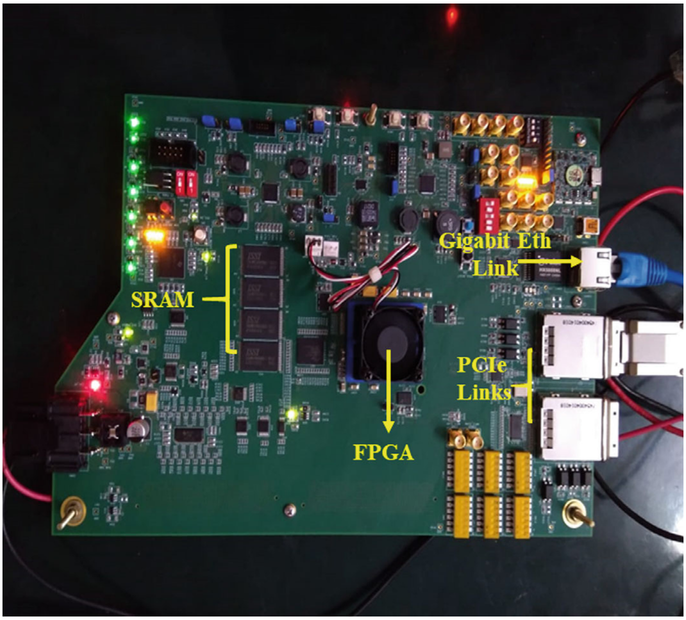

Fig. 4 Ultrasound receive hardware

Fig. 5 Ultrasound receive hardware integrated with system prototype

frequency data to the FPGA-based receive signal processing board. A fast Gigabit Ethernet link is used to process and stream the data that the transceiver hardware has received to the PC. The PC is then used for image generation and post-processing. The phantom image created by the developed system prototype is shown in Fig. 6.

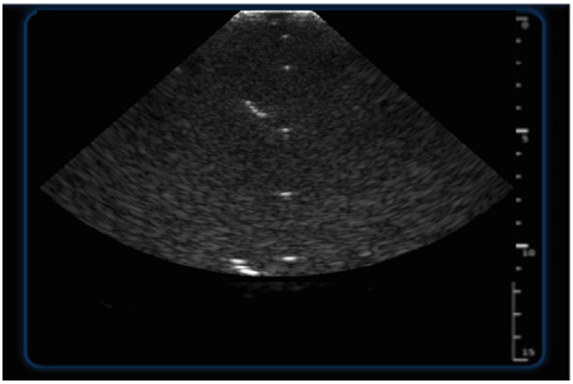

Fig. 6 Generated wire-phantom image by system prototype

5 Discussions

Much of the progress in ultrasound hardware development focuses on Open Ultrasound platforms tailored for research purposes [7]. Three crucial technical features that are necessary for open ultrasound platforms are given priority in these designs: high-throughput IO capabilities for real-time processing, generous memory for accessing pre-beamformed data, programmable TX operations on a per-channel basis, and an abundance of computational resources [8, 25, 26]. The integrated hardware components of several hardware-based open platforms were analyzed and analyzed [11, 26]. Power modules (High Voltage, Low Voltage) are separate, Transmitter section and backend processing based on FPGA or PC/GPU are commonly included in these systems. FPGA-based receive digital beamforming is frequently used in most systems because to the significant data bandwidth requirements [15, 16]. Evaluation board-based designs are explored through an analysis of current FPGA-based ultrasound imaging system designs. A programmable 128-channel FPGA-based solution with integrated power supplies, sequencing, and management is provided by this method [12]. Additionally, 512 Mb SRAM and 256 Mb QSPI Flash are built into the created circuitry. Board to Board, PCIe, and Gigabit Ethernet external interface connectors make it easier to link the created hardware to PCs and ultrasonic transceiver boards. The power tree is designed to use a single 12 V power supply to meet all of the power supply needs. During the circuits' peak functioning, the designed hardware is expected to need about 26W of power. For testing, test procedures and PC-based automation control were created. Additionally, the developed platform was integrated with the system prototype to assess the generated image quality.

6 Conclusions

A hardware platform, based on FPGA and designed to be reconfigurable, has been developed to execute the ultrasound receive signal processing chain. This platform incorporates a 128-channel digital beamformer, as well as PCIe and Gigabit Ethernet controllers, and has been interfaced with a PC for additional backend processing and display functionalities. By utilizing this reconfigurable platform, an ultrasound imaging system prototype was created and its imaging performance thoroughly assessed. The developed hardware platform holds potential for exploring the hardware implementation of ultrasound receive signal processing algorithms and conducting performance evaluations.

In contrast to previously reported efforts, this development constitutes a comprehensive 128-channel ultrasound receive signal processing hardware solution. Additionally, a 128-channel transceiver hardware was developed to seamlessly integrate with the reconfigurable platform, resulting in a holistic 128-channel "ultrasound prototype" solution. Analysis of the sensor-to-display signal chain in prototype systems indicates that the imaging performance is on par with commercial ultrasound imaging systems.

Acknowledgements "The Ministry of Electronics and Information Technology, Government of India, provided support for this work through the Medical Electronics and Health Informatics (ME & HI) Division in accordance with order No.1(5)/2015-ME&HI dated 18/11/2015 under the ICDU Project, and the Microelectronics Division in accordance with order No.9 (1)/2014-MDD dated 15-12-2014 under the SMDP-C2SD Project".

References

1. Aya I, Shuping Z, Federico A et al (2018) Towards ultrasound everywhere: a portable 3D digital back-end capable of zone and compound imaging. IEEE Trans Biomed Circ Syst 12(5):968–981
2. Kidav J et al (2022) Design of a128-channeltransceiver hardware for medical ultrasound imaging systems. IET Circ Dev Syst 16(1):92–104. https://doi.org/10.1049/cds2.12087
3. Kidav JU, Sivamangai NM, Pillai MP, Subash RM (2019) Architecture and FPGA prototype of cycle stealing DMA array signal processor for ultrasound sector imaging systems. Microprocess Microsyst 64:53–72
4. Kidav JU, Pavan ASR, Rajesh M, N KW (2022) A PC based ultrasound back-end signal processor using Intel® performance primitives. In: 2022 35th international conference on VLSI design and 2022 21st international conference on embedded systems (VLSID), Bangalore, India, pp 11–15. https://doi.org/10.1109/VLSID2022.2022.00015
5. Kidav JU (2022) An FPGA-accelerated parallel digital beamforming core for medical ultrasound sector imaging. IEEE Trans Ultrason Ferroelectr Freq Control 69(2):553–564. https://doi.org/10.1109/TUFFC.2021.3126578
6. Kim GD, Yoon C, Kye SB, Lee Y, Kang J, Yoo Y, Song TK (2012) A single FPGA-based portable ultrasound imaging system for point-of-care applications. IEEE Trans Ultrason Ferroelectr Freq Control 59(7):1386–1394
7. Boni E, Alfred CHY, Steven F, Arendt J, Tortoli P (2018) Ultrasound open platforms for next-generation imaging technique development. IEEE Trans Ultrason Ferroelectr Freq Control 65(7):1078–1092
8. Kidav JU, Sreejeesh SG, Navin Kumar W (2023) An FPGA implementation of gigabit Ethernet data transfer scheme for ultrasound imaging. In: Singh SN, Mahanta S, Singh YJ (eds) Proceedings of the NIELIT's international conference on communication, electronics and digital technology. NICE-DT 2023. Lecture notes in networks and systems, vol 676. Springer, Singapore. https://doi.org/10.1007/978-981-99-1699-3_21
9. Keenan C, Marcus LG (2016) Analysis of existing designs for FPGA-based ultrasound imaging systems. Int J Signal Process Image Process Pattern Recogn 9(7):13–24
10. Boni E et al (2012) A reconfigurable and programmable FPGA-based system for non standard ultrasound methods. IEEE Trans Ultrason Ferroelectr Freq Control 59(7):1378–1385
11. Boni E, Bassi L, Dallai A et al (2016) ULA-OP 256: a 256-channel open scanner for development and real-time implementation of new ultrasound methods. IEEE Trans Ultrason Ferroelectr Freq Control 63(10):1488–1492
12. Assef AA, Maia JM, Schneider FK, Eduardo TC, Vera LSNB (2012) Design of a 128-channel FPGA-based ultrasound imaging beamformer for research activities. In: Proceedings of the international ultrasonics symposium, Dresden, Germany, pp 635–638
13. Ricci S, Boni E, Guidi F, Morganti T, Tortoli P (2006) A programmable real-time system for development and test of new ultrasound investigation methods. IEEE Trans Ultrason Ferroelectr Freq Control 53(10):1813–1819

14. Assef AA, Maia JM, Costa ET (2015) A flexible multi-channel FPGA and PC-based ultrasound system for medical imaging research: initial phantom experiments. Res Biomed Eng 31(3):277–281
15. Sreejeesh SG, Sakthivel R, Kidav JU (2019) Beamforming algorithm architectures for medical ultrasound. Int J Innov Technol Explor Eng (IJITEE) 8(12). https://doi.org/10.35940/ijitee.L2556.1081219. ISSN:2278–3075
16. Sreejeesh SG, Sakthivel R, Kidav JU (2024) Various ultrasound beamformer designs and architectures: an update. Theory Appl Eng Res 7:64–83. https://doi.org/10.9734/bpi/taer/v7/2916G
17. Sreejeesh SG, Sakthivel R, Kidav JU (2020) Superior implementation of accelerated QR decomposition for ultrasound imaging. IEEE Access 8:156244–156260. https://doi.org/10.1109/ACCESS.2020.3017558
18. Kidav JU, Sivamangai DNM, Pillai DMP, Sreejeesh SG (2019) Design and physical implementation of array signal processor ASIC for sector imaging systems. In: 2019 32nd international conference on VLSI design and 2019 18th international conference on embedded systems (VLSID), Delhi, India, pp 448–453. https://doi.org/10.1109/VLSID.2019.00095
19. Kidav JU, Sivamangai NM, Pillai MP, Sreejeesh SG (2021) A broadband MVDR beamforming core for ultrasound imaging. Integr VLSI J 81:221–233
20. Hema N, Kidav JU, Lakshmi B (2015) VLSI architecture for broadband MVDR beamformer. Indian J Sci Technol 8:19
21. Kidav JU, Salma AS (2023) Design and development of POSIT arithmetic-based digital beamformer for ultrasound imaging system. Int J Digit Technol 2(2)
22. Kidav JU, Siva Mangai NM, Pillai MP (2020) Design of AWC core using DCD iterations for MVDR beamformer. Microprocess Microsyst 73:102969. ISSN 0141–9331. https://doi.org/10.1016/j.micpro.2019.102969
23. Kidav JU, Mohan V (2023). esign and development of an FPGA-based real-time reconfigurable computing platform. In: Singh SN, Mahanta S, Singh YJ (eds) Proceedings of the NIELIT's international conference on communication, electronics and digital technology. NICE-DT 2023. Lecture notes in networks and systems, vol 676. Springer, Singapore. https://doi.org/10.1007/978-981-99-1699-3_24
24. 7 Series FPGAs Data Sheet: Overview. Xilinx® 2020
25. Vijitha CV, Najla AP, Kidav JU (2014) PCI express interface development and simulation for high speed data transmission. (IJCSIT) Int J Comput Sci Inform Technol 5(2):2574–2577
26. Kidav JU, Rajesh M, Sreejeesh SG, Kumar P, Kumar N, Vinisha P (2024) Design of a digital receive beamformer ASIC based ultrasound imaging system prototype. J Circ Syst Comput. https://doi.org/10.1142/S0218126625500641