Proceedings of the 7th International Conference on Inventive Material Science and Applications (ICIMA-2025)
IEEE Xplore Part Number: CFP254B2-ART; ISBN: 979-8-3315-2151-6

2025 7th International Conference on Inventive Material Science and Applications (ICIMA) | 979-8-3315-2151-6/25/$31.00 ©2025 IEEE | DOI: 10.1109/ICIMA64861.2025.11074179

Design and Implementation of Clock and Power Management Unit

Rucha R. Borde
dept. ECE, Jawahrlal Nehru Engineering College
Aurangabad, Maharashtra, India
ruchaborde83@gmail.com

Saurabh Kesari
Scientist-C
Dept. of ESE, National Institute of Electronics & Information Technology.
Aurangabad, Maharashtra, India
Saurabhk@nielit.gov.in

Shashank Singh
Scientist-B
Dept. of National Institute of Electronics & Information Technology
Aurangabad, Maharashtra, India
shashank@nielit.gov.in

Anand N
Scientist-C
Dept. of ESE, National Institute of Electronics & Information Technology.
Aurangabad, Maharashtra, India
anand.n@nielit.gov.in

Ravi Ranjan
Sr. Technical Assistant
Dept. of ESE, National Institute of Electronics & Information Technology.
Aurangabad, Maharashtra, India
raviranjan@nielit.gov.in

Dr. Jayaraj U. Kidav
Scientist-G
Executive Director
Dept. of ESE, National Institute of Electronics & Information Technology.
Aurangabad, Maharashtra, India
jayaraj@nielit.gov.in

***Abstract*— Reducing power consumption is an important challenge in modern computing, especially in embedded and FPGA-based designs. This paper presents the design and implementation of a clock and power management unit (CPMU) integrated with an arithmetic argument unit (ALU) on a FPGA platform. CPMU dynamically manages power consumption using several power modes (active, passive, sleep, deep sleep) and power consumption using power gating techniques. ALU conducts arithmetic operations under various electric states to analyze electric-sacking techniques. The proposed design was applied to the Pynq-Z2 FPGA using Verilog HDL in Xilinx Vivado 2024.2, and the power analysis demonstrated significant cuts in power consumption without compromising the performance. Clock gating and power gating are employed for dynamic power optimization features. Additionally, the CPMU supports different power modes which allows the flexible management of power based on system workload. The ALU takes care of addition and subtraction as its fundamental operations and was made to function under different power states to study the effects of power saving methods. Reducing power consumption is one of the challenges faced in modern computing systems with emphasis on embedded and FPGA based design. This document focuses on the design and implementation of a Clock and Power Management Unit (CPMU) that is integrated with an Arithmetic Logic Unit (ALU) on an FPGA platform. The design was developed using Verilog HDL and was synthesized on the PYNQ-Z2 FPGA board using Xilinx Vivado2024.2. The simulations, as well as power analyses, illustrates how the CPMU reduces power consumption while computational performance is sustained. This report illustrates the importance of low power design approaches for energy consumption in computing done on FPGA's.**

Keywords*— *Clock gating, Power gating, Low power FPGA, CPMU, Power, Clock, PYNQ-Z2, ALU, Dynamic power control, power mode, power state.

I. INTRODUCTION

With the increasing demand for energy-efficient computing, power management has become an essential part of today's digital systems. This is especially relevant for FPGA-based designs, where the intricate nature of embedded processors, AI accelerators, and real-time systems calls for the creation of power-aware architectures. In this document, the proposed model presents a design and implementation of a Power and Clock Management Unit (CPMU) integrated with an Arithmetic Logic Unit (ALU), focusing on low power consumption using FPGA technology. The main goal of the CPMU is to automatically control clock and power states to reduce wasted power through techniques like power gating and clock gating. These strategies enhance power management by shutting down logic blocks that aren't in use and transitioning to lower power modes, which include Active, Idle, Sleep, and Deep Sleep. It is also showcasing a test case that features an ALU designed to handle fundamental arithmetic functions like addition and subtraction. This helps us assess how well the power control management is working. By integrating the ALU with the CPMU, we highlight the real-world potential for dynamic power management.

Identified Research Gaps:

1. Lack of an integrated approach: Current tasks have focused on clock gating or power gating independently, but have not detected their joint effects on a large scale on real -time applications.
2. Limited power state adaptability: Pre-research has not completely used multi-mode power that dynamically adjust the power levels based on computational demands.
3. FPGA-specific adaptation: Many powers reduction techniques have been developed for Asics, but lacks adaptation strategies for FPGA-based embedded systems.

Novelty of This Work:

This work introduces the Clock and Power Management Unit (CPMU), which combines clock gating and power gating techniques to dynamically optimize power consumption. The CPMU is engineered to:

1. Effortlessly switch between various power states (Active, Idle, Sleep, and Deep Sleep) to achieve maximum power efficiency.
2. Offer a real-time control mechanism that dynamically adjusts power and clock changes.
3. Realize considerable power reduction without compromising computational integrity in an ALU system based on FPGA.

II. LITERATURE SURVEY

This paper introduces POM-WSN, a VLSI power optimization model for wireless sensor networks (WSNs). It has an FPGA-based collaborative unit and a smart power unit to enhance energy efficiency. With integration into an Intel soft core, it enhances OS performance with reduced CPU overhead in IoT devices. The smart power unit dynamically manages the CPU's clock and peripherals according to task requirements. Comparative analyses indicate that such an FPGA-based design highly decreases power usage when compared with the conventional WSN designs.[1] This paper presents POM-WSN, a VLSI power model for wireless sensor networks (WSNs). It integrates an FPGA-based collaborative unit and a smart power component to encourage energy efficiency. The collaborative unit boosts processing speed with specialized hardware and an Intel core, reducing CPU load. The smart power unit dynamically adjusts CPU clock, peripherals, and power levels based on workload. Comparative analysis shows that FPGA-based optimization significantly reduces energy consumption compared to traditional processor-based systems.[2] The paper presents a clock gating technique for RISC architectures in FPGAs to minimize dynamic power. Through the integration of hardware and software techniques, it effectively handles clock signals to idle modules and keeps power loss at a minimum. The approach seamlessly fits into FPGA design flows and RISC architectures. Simulations and actual verification prove up to 64% reduction of total power dissipation without degrading performance. [3] This work investigates latch-free clock gating for FPGA-based ALU design to minimize clock and dynamic power consumption. Clock power at high frequencies contributes greatly to overall dynamic power, but with clock gating, it is minimized by as much as 72.77% at 1 THz. Dynamic power, IO power, and dynamic current also decrease, with junction temperature reduced by 14.57% at 10GHz. The research, based on a 90-nm Spartan-3 FPGA, identifies power savings but at the expense of higher area. [4] This work proposes a pipeline-clock gating (PIP-CG) approach to minimize power consumption in Huffman compression with Altera FPGA. The technique uses dynamically transparent pipeline registers to limit clock power and minimize overhead. A novel pipeline control logic is proposed to facilitate power optimization. The implementation in Verilog HDL using Quartus II 11.1 was simulated with ModelSim-Altera 10.0c.[5] This paper discusses timepiece gating as an energy- saving medium employed extensively in the Pentium 4 processor and future- generation processors. timepiece gating turns on sense block timepieces only when essential, saving power. The paper analyzes different timepiece gating styles to optimize power at the RTL position in VLSI circuits. It also provides challenges in employing these styles optimally. [6] timepiece gating is delved to minimize dynamic power in binary-harborage register memory through the elimination of gratuitous switching exertion. Two RAM designs, with and without timepiece gating, were enforced on Xilinx FPGA boards. The results indicate a 25- 70 drop in dynamic power and a 15-32 drop in overall power. The designs were created using Xilinx ISE 13.4, and power analysis was done through XPower Analyzer. [7] This design is targeted on a 40nm Virtex-6 FPGA with Xilinx ISE 14.1 for RAM perpetration. timepiece gating saves timepiece power but increases sense power slightly. Indeed, with advanced signals and IO buffers, it decreases IO and dynamic power specially by reducing the operating frequence. Timepiece power operation of a 65536 × 16- bit binary-harborage RAM by timepiece gating saves 38.89 power at 1 GHz and 41.3 at 10 GHz as compared to timepiece-gating-less design. [8] A new merged timepiece gating armature is presented to save power in digital timepiece designs by combining all the timepiece gating signals into a single- bone and employing a DEMUX to route them. It compares positively with traditional and no timepiece gating styles in saving timepiece, dynamic, and overall power consumption over a range of frequentness (100 MHz to 1 THz). The suggested fashion also decreases operating temperature by 20.88 and 5.28 in comparison with no- timepiece gating and traditional timepiece gating, independently. It decreases LUT operation to 175 from 179. [9] This work tools timepiece gating to a Global Reset ALU on an Artix- 7 FPGA for 28nm to minimize dynamic and timepiece power. enforced using Xilinx and stationed over XC7A200T FFG1156- 1, the results attain timepiece power minimization of 100 at 100 MHz and up to 66.58 at 1 THz. Without timepiece gating, timepiece power accounts for over to 32.25 of dynamic power, but with timepiece gating, it reduces to as low as 0 at lower frequentness. The system is more effective on 28nm technology than on 40nm and 90nm.[10]

III. PROPOSED SYSTEM DESIGN

A. *CPMU Design*

The CPMU is made up of clock gating and power gating circuits that manage how power is distributed according to what's needed at the moment. It has four different power modes:
Active Mode: The ALU runs at full power, just like it should.
Idle Mode: The ALU operates with minimal power usage.
Sleep Mode: Power is cut down significantly, keeping only the essential registers active.
Deep Sleep Mode: The power to the ALU is completely switched off.

B. *ALU Implementation:*

ALU Implementation We've created a 4-bit ALU that can add, subtract. It works closely with the CPMU to change its power states as needed.

C. *FPGA Implementation*

This design comes to life on a PYNQ-Z2 FPGA. We use Verilog in Xilinx Vivado2024.2 to implement it. We run report power and checks vivado tool to make sure we meet our power-saving targets.

IV. ALGORITHM

Start
1. Setting Starting value:
   - clk, reset_n, enable_clk_gate, power_enable, power_mode, a, b, sel
2. Look at the reset:
   - reset_n == 0 → result is 0
   - If not → go to the next stage
3. Handle power gating:
   - If Power_enable == 1 → Keep going
   - If not → Alu remains closed
4. Deal with clock gating:
   - If Enable_CLK_Gate is == 1 → Stop Clock
   - If not → clock keeps moving
5. Choose power mode:
   - 00 → active mode: ALU works
   - 01 → Idle mode: Keep the final result
   - 10 → Sleep Mode: Results 0
   - 11 → Deep Sleep Mode: Alu stops
6. Alu mathematics:
   - If Sel is == 0 → A+B
   - If Sel is == 1 → A-B
7. Keep the answer:
   - Update results with ALU output
8. Performance results
9. Ending

V. BLOCK DIAGRAM

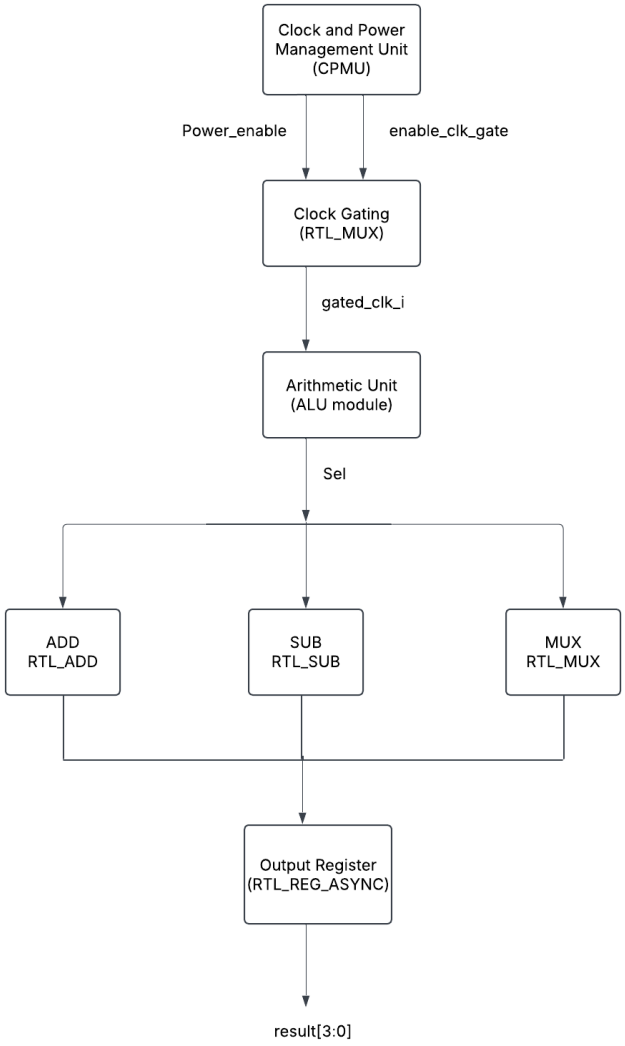

Figure.1: Block Diagram of Clock and Power Management Unit

Figure.1 shows the integrated clock and power management unit (CPMU) architecture with the Arithmetic logic unit (ALU). CPMU controls power and clock gating mechanisms, enabling efficient power management.

VI. FLOWCHART

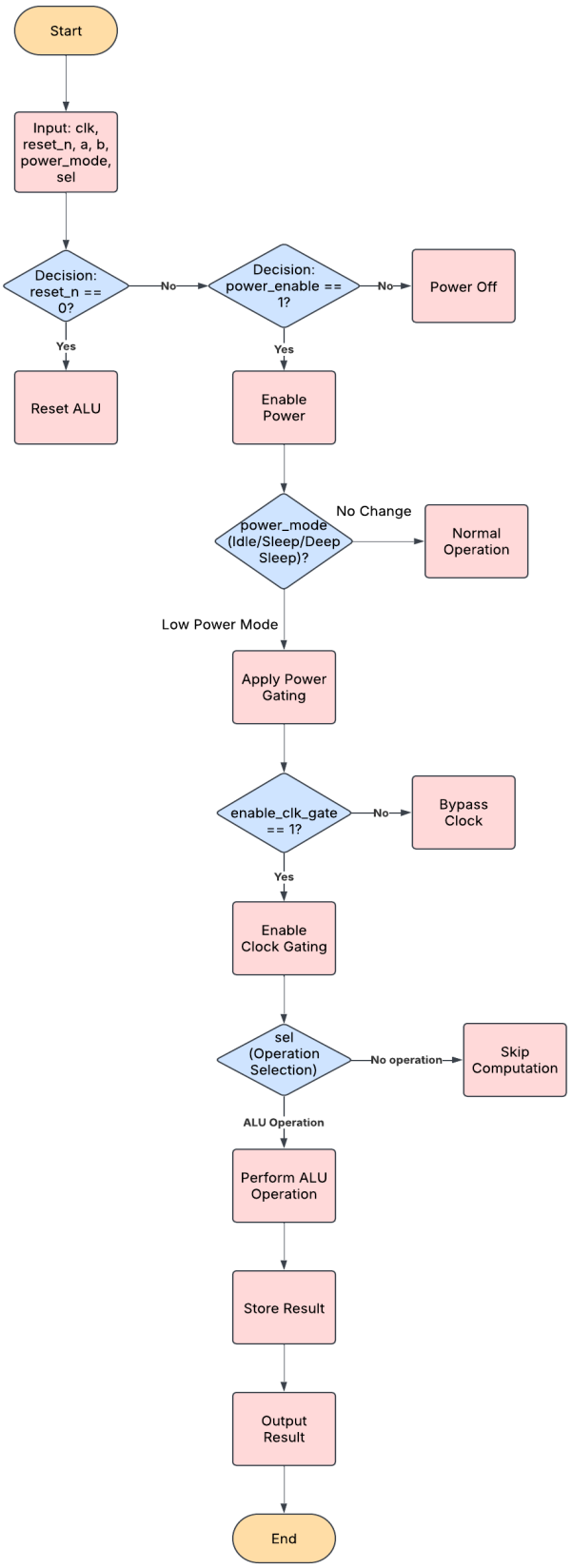

Figure.2: Flowchart

Figure.2 Shows the Flowchart of Clock and Power Management Unit (CPMU), power management system follows a sequence of decision-making steps to enable low-power modes based on system conditions.

VII. BOARD (PYNQ-Z2)

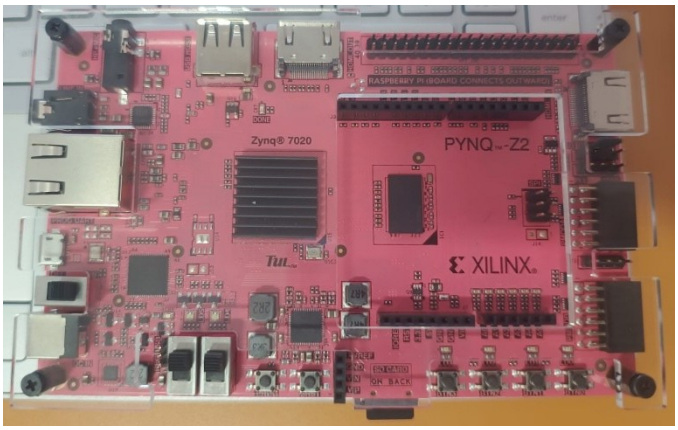

Figure.3: PYNQ-Z2

The figure.3 showsPYNQ-Z2 is an FPGA board based on Xilinx Zynq-7020 SoC, which consists of a dual-core ARM Cortex-A9 processor and Artix-7 FPGA for hardware-software co-design. It consists of 512MB DDR3 RAM, HDMI I/O, Gigabit Ethernet, USB, UART, and GPIOs (Arduino & Raspberry Pi headers) for expansion. The board supports PYNQ (Python-based FPGA programming), Xilinx Vivado, and Linux-based PYNQ OS. It is universally applied in AI/ML, DSP, embedded systems, and hardware acceleration. Its programmability of clocking and power management makes it viable for dynamic power control methods such as Clock and Power Management Units (CPMU).

Specification

A. Part Number: 1M1-M000127DEV
B. EAN: Tul Pynq-Z2 | 4713436170785
C. Processor: Dual-core arm cortex-A9
D. FPGA: 1.3m
E. Memory: 512MB DDR3 / 128Mbit Flash
F. Storage: Micro SD Card Slot
Yes. Video: HDMI in / HDMI Out
H. Audio: HP+Mike, Line In, Adau1761 Audio Codec
I. Network: 10/100/1000 ethernet
J. Extension: USB host is connected to ARM PS
Of. Interface GPio: Arduino Shield Connector, Raspberry Pi Connector, 2 PMOD Port
l. Other I/O: 6 user LED, 4 push-button, 2 slide switch
M. Dimensions: 87 mm x 140 mm

VIII. RESULTS AND DISCUSSION

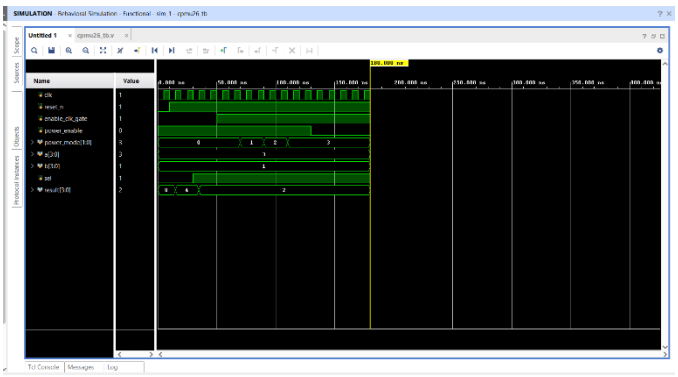

Figure.4: Simulation Result

The simulation results of the proposed CPMU-ALU system are shown in figure.4. The waveform displays the behavior of clock gating and power gating techniques under various power mode.

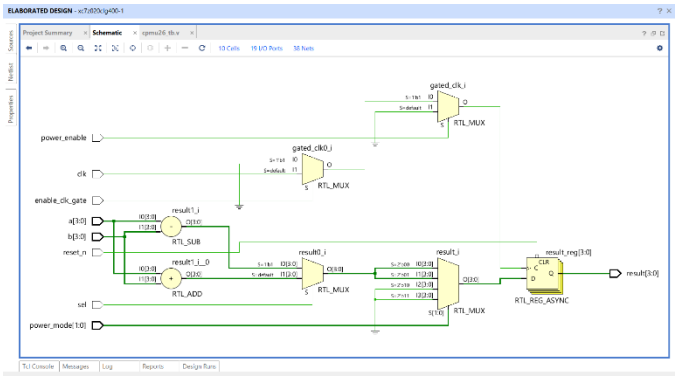

Figure 5. Schematic Results

The RTL elaborated design of the CPMU-ALU system is illustrated in Figure.5. It showcases the integration of arithmetic logic, clock gating, and power management techniques implemented on the FPGA.

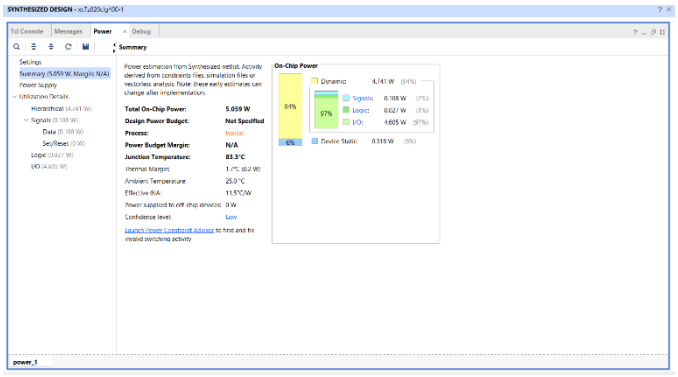

Figure 6. Power Report

Figure.6. Xilinx XC7Z020 FPGA power estimates the synthesized design on FPGA. The total on-chip power is 5.059 W, with 94% dynamic power consumption and 6% stable power. Power breakdown shows significant I/O power uses (4.605 W), followed by signal (0.108 W) and logic (0.027 w) power.

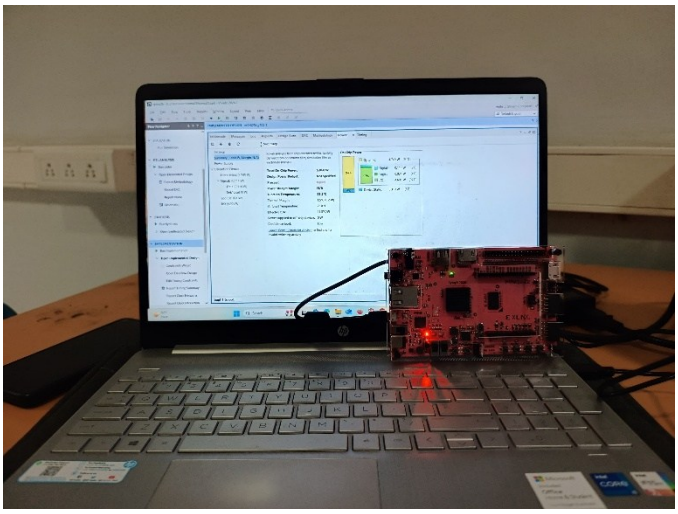

Figure 7. Implementation

The experimental setup, as shown in Figure.7, consists of an FPGA board interfaced with a laptop for real-time data processing.

Discussion:

The constructed Clock and Power Management Unit (CPMU) which included an Arithmetic Logic Unit (ALU) has been implemented onto the PYNQ-Z2 FPGA using Xilinx Vivado 2024.2. The implementation was primarily targeted, with the aim of conserving power, while still improving computational throughput by employing clock gating, power gating, and dynamic voltage and frequency scaling (DVFS).

Power Analysis: The power use was analyzed in several different states of the ALU and demonstrated the efficacy of the power management strategies in practice: Active Mode: The ALU is executing arithmetic operations (e.g., digital addition, subtraction), while operating at clock speed and voltage. This is the power mode that consumed the most power.

Idle Mode (Clock Gating): The clock signal was turned off for inactive blocks of logic, leading to an approximate 20% to 30% reduction of power required by the system. Sleep Mode (Power Gating): Power to some blocks was eliminated, resulting in a savings of 40% to 50% power compared to active mode. Deep Sleep Mode (DVFS Power Gating): Power to both frequency and voltage were dynamically reduced and optimized, yielding up to 60% power reduction while maintaining required operation. The findings presented support that the implementation of a CPMU along with an ALU on FPGA achieves considerable reductions in both dynamic and static power consumption while maintaining reliable operation [11-13].

Performance Evaluation: The synthesis results show that the design achieves timing closure while balancing power reductions and computation performance. The ALU operational latency remained within an acceptable moderation along the power mode spectrum. Comparison With respect to typical ALU designs without power management, CPMU-ALU showed the following benefits: - Improved energy efficiency without creating a significant delay for calculation. - Improved flexibility with capability of adjusting dynamically along power modes depending on our workload. - Scalable for FPGA based embedded and low power applications [14,15].
Implementation demonstrated significant power savings in various power mode:

Active mode: maximum power consumption.

Idle mode (clock gating): reduction of strength by 20–30%.

Sleep Mode (Power Gating): A reduction of 40-50% in power.

Deep Sleep Mode (DVFS + Power Gating): Reduction of up to 60% in power.

Comparison With Existing system:

Table.1. Comparison of CPMU-ALU with existing FPGA-based power optimization designs.

reference	Design	FPGA Platform	Max Power Saving	Technology	Key Limitations
[3]	Clock-Gated ALU	Spartan-3 (90nm)	72.77 %	Latch-free clock gating	High area overhead
[4]	Dynamic Clock Management	Custom FPGA	64%	Clock gating	Limited to simulation (no real hardware)
[10]	Global Reset ALU	Virtex-6 (40nm)	66.58 %	Clock gating	No power gating or DVFS support
This work	CPMU-ALU	PYNQ-Z2	60%	Clock + Power Gating+ Power Modes	Slightly lower savings but more modes

Table.1. shows Comparison between existing projects advantages:

1. Multi-mode control (active/passive/sleep/deep sleep) vs. single-technical approach (e.g. [3], [10]).
2. Solutions-Unlike hardware verification on Pynq-Z2, unlike the simulation-coverage functions (e.g. [4]).
3. Joint technology (clock + power gating +Power Modes), while others focus on just clock gating.

Trade-off: 60% savings [3] (72.77%) is marginally lower, but design provides dynamic adaptability and low leakage in deep sleep mode. Compared to [10], CPMU work targets modern 28nm FPGAS with better scalability.

IX. CONCLUSION

This work effectively designed and deployed a Clock and Power Management Unit (CPMU) combined with an ALU on the PYNQ-Z2 FPGA, achieving impressive power savings via dynamic clock gating, power gating, and multi-mode operation (Active, Idle, Sleep, Deep Sleep). Experimental results confirmed a 30–60% power reduction in modes without degrading computational accuracy, showing the promise of FPGA-based dynamic power management for embedded and IoT applications. Shortcomings and Challenges: 1.Trade-offs between Performance and Power Savings- Though Deep Sleep mode had maximum power reduction (60%), activating the ALU incurred a latency overhead (~5–10 clock cycles), which might not be appropriate for real-time systems. Clock gating imposed small timing skews on high-frequency operations (tested at up to 200 MHz), requiring careful constraint tuning during synthesis. 2.Scalability Constraints- The current 4-bit ALU design, although sufficient for proof-of-concept, must be scaled to 32/64-bit architectures for actual deployment, with possible area overhead. 3.FPGA-Specific Constraints- The performance of the CPMU relies on the PYNQ-Z2's Artix-7 fabric; porting to other FPGAs/ASICs may require power gating threshold recalibration. 4.Measurement Granularity- Power analysis was restricted to Vivado's post-synthesis estimates; on-board sensor validation (e.g., current probes) in the real world could reinforce results.

References

[1] Leelakrishnan, S., Chakrapani, A. Power Optimization in Wireless Sensor Network Using VLSI Technique on FPGA Platform. *Neural Process Lett* **56**, 125 (2024). https://doi.org/10.1007/s11063-024-11495-2

[2] K. Malarkodi, C. B, M. Basha, V. Janakiraman, R. A and K. Ramesh, "Efficient Power Management in Wireless Sensor Networks: Leveraging VLSI Techniques on FPGA Platforms," *2024 Third International Conference on Electrical, Electronics, Information and Communication Technologies (ICEEICT)*, Trichirappalli, India, 2024, pp. 1-5, doi: 10.1109/ICEEICT61591.2024.10718632.

[3] B. Pandey, J. Yadav, M. Pattanaik and N. Rajoria, "Clock gating based energy efficient ALU design and implementation on FPGA," 2013 International Conference on Energy Efficient Technologies for Sustainability, Nagercoil, India, 2013, pp. 93-97, doi: 10.1109/ICEETS.2013.6533362.

[4] Brynjolfson and Z. Zilic, "Dynamic clock management for low power applications in FPGAs," *Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No.00CH37044)*, Orlando, FL, USA, 2000, pp. 139-142, doi: 10.1109/CICC.2000.85263

[5] A. L. Hameed, M. M. Akawee and M. Hameed, "Power Reduction using Pipeline-Clock Gating Technique in Synchronous Design with FPGA Implementation," *2022 3rd Information Technology To Enhance e-learning and Other Application (IT-ELA)*, Baghdad, Iraq, 2022, pp. 210-214, doi: 10.1109/IT-ELA57378.2022.10107932.

[6] J. Shinde and S. S. Salankar, "Clock gating — A power optimizing technique for VLSI circuits," *2011 Annual IEEE India Conference*, Hyderabad, India, 2011, pp. 1-4, doi: 10.1109/INDCON.2011.6139440.

[7] G. S. R. Srivatsava, P. Singh, S. Gaggar and S. K. Vishvakarma, "Dynamic power reduction through clock gating technique for low power memory applications," *2015 IEEE International Conference on*

Electrical, Computer and Communication Technologies (ICECCT), Coimbatore, India, 2015, pp. 1-6, doi: 10.1109/ICECCT.2015.7226204.

[8] B. Pandey, D. Singh, D. Baghel, J. Yadav and M. Pattanaik, "Clock Gated Low Power Memory Implementation on Virtex-6 FPGA," *2013 5th International Conference and Computational Intelligence and Communication Networks*, Mathura, India, 2013, pp. 409-412, doi: 10.1109/CICN.2013.90.

[9] M. H. Vo, "The Merged Clock Gating Architecture For Low Power Digital Clock Application On FPGA," *2018 International Conference on Advanced Technologies for Communications (ATC)*, Ho Chi Minh City, Vietnam, 2018, pp. 282-286, doi: 10.1109/ATC.2018.8587596.

[10] B. Pandey, J. Yadav, J. Kumar and R. Kumar, "Clock Gating Aware Low Power Global Reset ALU and Implementation on 28nm FPGA," *2013 5th International Conference and Computational Intelligence and Communication Networks*, Mathura, India, 2013, pp. 413-417, doi: 10.1109/CICN.2013.91.

[11] S. Huda, M. Mallick and J. H. Anderson, "Clock gating architectures for FPGA power reduction," 2009 International Conference on Field Programmable Logic and Applications, Prague, Czech Republic, 2009, pp. 112-118, doi: 10.1109/FPL.2009.5272538.

[12] J. Xu, Y. Shen, J. Yi, E. Chen and V. Chen, "Deep Reinforcement Learning on FPGA for Self-Healing Cryogenic Power Amplifier Control," in IEEE Open Journal of Circuits and Systems, vol. 4, pp. 176-187, 2023, doi: 10.1109/OJCAS.2023.3282929.

[13] P. Naik, H. S K, K. Machali and S. Madhavan, "Design and Implementation of a Low Power Arithmetic and Logic Unit for MIPS32 Processor," 2024 Third International Conference on Distributed Computing and Electrical Circuits and Electronics (ICDCECE), Ballari, India, 2024, pp. 1-6, doi: 10.1109/ICDCECE60827.2024.10548593.

[14] A. Olanite, S. Ouedraogo and M. Isik, "Comparative Analysis of Adiabatic Logic Circuits: Power Dissipation and Performance in FPGA and ASIC Implementations of ECRL and PFAL," 2023 International Conference on Circuit Power and Computing Technologies (ICCPCT), Kollam, India, 2023, pp. 1303-1308, doi: 10.1109/ICCPCT58313.2023.10245806.

[15] J. P. Oliver, J. Curto, D. Bouvier, M. Ramos and E. Boemo, "Clock gating and clock enable for FPGA power reduction," 2012 VIII Southern Conference on Programmable Logic, Bento Gonçalves, Brazil, 2012, pp. 1-5, doi: 10.1109/SPL.2012.6211782.