Semester I

Discipline: ELECTRONICS & COMMUNICATION ENGINEERING

Stream: EC8

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221TEC100	ADVANCED ENGINEERING MATHEMATICS	DISCIPLINE CORE	3	0	0	3

Preamble: The purpose of this course is to expose students to the basic theory of linear algebra and probability.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs. After the completion of the course the student will be able to

CO 1	To analyze distributions of random variables and make computations based on that
CO 2	evaluate average behaviour of random variables, and analyze their converging behviours
CO 3	To analyze behaviour of random processes and explain basis of vector spaces.
CO 4	To evaluate properties of linear transformations
CO 5	To evaluate if a linear tranformaion is diagonalizable and decompose it using spectral decomposition theorem.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO4	PO5	PO6	PO7
CO 1	3		3		3	3	
CO 2	3		3		3	3	
CO 3	3		3		3	3	
CO 4	3		3		3	3	
CO 5	3		3		3	3	

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	20
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation: 40 marks

- Problem assignments including unsolved exercise problems from reference text books: 20 marks
- Quiz: 10 marks
- Test paper (1 number): 10 marks

Quiz shall include topics from at least 50% of the syllabus. Test paper shall include minimum 80% of the syllabus

End Semester Examination Pattern:

End Semester Examination: 60 marks

There will be two parts; Part A and Part B

- Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions.
- Part B will contain 7 questions with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

A P J ABDUL KALAM TECHNOLOGICAL UNIVERSITY
M.TECH DEGREE EXAMINATION
SEMESTER:
Branch:
ADVANCED ENGINEERING MATHEMATICS

Time: 2.5 Hours **Marks: 60**

Part A

Answer ALL Questions. Each question carries 5 marks

1. Given that $f(x) = \frac{k}{2^x}$ is a probability distribution of a random variable that can take on the values $x = 0,1,2,3,\wedge 4$. Find k. Find the cumulative distribution function.
2. State and prove weak law of large numbers.
3. Show that $(1,3,2,-2), (4,1,-1,3), (1,1,2,0), (0,0,0,1)$ is a basis for R^4.
4. Let $T: V \to W$be a linear transformation defined by $T(x,y,z) = (x+y, x-y, 2x+z)$. Find the range, null space, rank and nullity of T.
5. Describe an inner product space. If V is an inner product space, then for any vectors α, βin V prove that $\|\alpha+\beta\| \leq \|\alpha\| + \|\beta\|$.

Part B

Answer ANY FIVE Questions, one from each module
(5 x 7 marks = 35marks)

6. If the probability mass function of a RV X is given by $P(X=x) = kx^3, x = 1,2,3,4$. Find the value of k, $P\left[\left(\frac{1}{2} < X < \frac{3}{2}\right)/X > 1\right]$,mean and variance of X.
7. If the moment generating function of a uniform distribution for a random variable X is $\frac{1}{t}(e^{5t} - e^{4t})$.Find E(X).
8. Consider the Markov chain with three states, s={1,2,3} that has the following transition matrix $P = \begin{bmatrix} \frac{1}{2} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{3} & 0 & \frac{2}{3} \\ \frac{1}{2} & \frac{1}{2} & 0 \end{bmatrix}$ Draw the state diagram for the chain. If $P(X_1 = 1) = P(X_2 = 2) = \frac{1}{4}$, find $P(X_1 = 3, X_2 = 2, X_3 = 1)$.
9. Find the eigen values and eigen vectors of $A = \begin{bmatrix} 2 & 2 & 1 \\ 1 & 3 & 1 \\ 1 & 2 & 2 \end{bmatrix}$.

10. Find the least square solution to the equation $Ax = b$, where $A = \begin{bmatrix} 1 & 2 \\ 1 & 3 \\ 0 & 0 \end{bmatrix}$ and $b = \begin{bmatrix} 4 \\ 5 \\ 6 \end{bmatrix}$, Obtain the projection matrix P which projects b on to the column space of A.
11. Let T be the linear transformation from R^3 to R^2 defined by T(x,y,z) =(x+y, 2z-x). Let B_1, B_2 be standard ordered bases of R^3 and R^2 respectively. Compute the matrix of T relative to the pair B_1, B_2.
12. Let V be a finite-dimensional complex inner product space, and let T be any linear operator on V. Show that there is an orthonormal basis for V in which the matrix of T is upper triangular.

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Syllabus

Module 1 Axiomatic definition of probability. Independence. Bayes' theorem and applications. Random variables. Cumulative distribution function, Probability Mass Function, Probability Density function, Conditional and Joint Distributions and densities, Independence of random variables. Functions of Random Variables: Two functions of two random variables. Pdf of functions of random variables using Jacobian.

Module 2 Expectation, Fundamental theorem of expectation, Moment generating functions, Characteristic function. Conditional expectation. Covariance matrix. Uncorrelated random variables. Pdf of Jointly Gaussian random variables, Markov and Chebyshev inequalities, Chernoff bound. Central Limit theorem. Convergence of random variables. Weak law of large numbers, Strong law of large numbers.

Module 3 Random Processes. Poisson Process, Wiener Process, Markov Process, Birth-Death Markov Chains, Chapman- Kolmogorov Equations,

Groups, Rings, homomorphism of rings. Field. Vector Space. Subspaces. direct sum. Linear independence, span. Basis. Dimension. Finite dimensional vector spaces. Coordinate representation of vectors. Row spaces and column spaces of matrices.

Module 4 Linear Transformations. Four fundamental subspaces of a linear transformation. Rank and Rank-nullity theorem. Matrix representation of linear transformation. Change of basis transformation. System of linear equations. Existence and uniqueness of solutions. Linear functionals. Dual, double dual and transpose of a linear transformation.

Module 5 Eigen values, Eigen vectors, Diagonizability.

Inner product. Norm. Projection. Least-squares solution. Cauchy-Schwartz inequality. Orthonormal bases. Orthogonal complement. Spectral decomposition theorem.

Course Plan

No	Topic	No. of Lectures
	Module I	
1.1	Axiomatic definition of probability. Independence. Bayes' theorem and applications.	2
1.2	Random variables. Cumulative distribution function, Probability Mass Function,	1
1.3	Probability Density function, Conditional and Joint Distributions and densities, Independence of random variables.	2
1.4	Functions of Random Variables: Two functions of two random variables. Pdf of functions of random variables using jacobian.	2
	Module II	
2.1	Expectation, Fundamental theorem of expectation, Conditional expectation.	1
2.2	Moment generating functions, Charectristic function.	1
2.3	Covariance matrix. Uncorrelated random variables. Pdf of Jointly Guassian random variables,	2
2.4	Markov and Chebyshev inequalities, Chernoff bound. Central Limit theorem.	2
2.5	Convergence of random variables. Weak law of large numbers, Strong law of large numbers.	2
3	**Module III**	
3.1	Random Processes. Poisson Process, Wiener Process,	2
3.2	Markov Process, Birth-Death Markov Chains, Chapman-Kolmogorov Equations,	2
3.3	Groups, Rings, homomorphism of rings. Field. Vector Space. Subspaces. direct sum.	2
3.4	Linear independence, span. Basis. Dimension. Finite dimensional vector spaces.	2
3.5	Coordinate representation of vectors. Rowspaces and column spaces of matrices.	1
4	**Module IV**	
4.1	Linear Transformations. Four fundamental subspaces of a linear transformation. Rank and Rank-nullity theorem.	2
4.2	Matrix representation of linear transformation. Change of basis transformation.	1
4.3	System of linear equations. Existence and uniqueness of solutions.	2
4.4	Linear functionals. Dual, double dual and transpose of a linear transformation.	2

5	**Module V**	
5.1	Eigen values, Eigen vectors, Diagonizability.	2
5.2	Inner product. Norm. Projection. Least-squares solution. Cauchy-Schwartz inequality.	2
5.3	Orthonormal bases. Orthogonal complement. Spectral decomposition theorem.	2

Reference Books

1. Hoffman Kenneth and Kunze Ray, Linear Algebra, Prentice Hall of India.

2. Jimmie Gilbert and Linda Gilbert, Linear Algebra and Matrix Theory, Elsevier

3. Henry Stark and John W. Woods "Probability and Random Processes withApplications to Signal Processing", Pearson Education, Third edition.

4. Athanasios Papoulis and S. Unnikrishna Pillai. Probability, Random Variables and Stochastic Processes, TMH

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221TEC001	SYSTEM DESIGN USING EMBEDDED PROCESSORS	Program Core	3	0	0	3

Preamble: Embedded systems are normally built around Microcontrollers and ARM Processor based SoCs. This Embedded System using Embedded Processors course focuses on the architecture and programming of embedded processors. The objective of the course is to provide understanding of the techniques essential to the design and implementation of embedded systems using suitable hardware and software tools. This course offers a range of topics of immediate relevance to industry and makes the participants exactly suitable for Embedded Industry

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Comprehend Embedded Processor and its software
CO 2	Design an Embedded system with ARM microcontrollers
CO 3	Design an Embedded system using processors, memory I/O devices and communication network within realistic constraints.
CO 4	Comprehend ARM Cortex M4 microcontrollers
CO 5	Comprehend the peripheral programming of ARm cortex M4 Microcontrollers
CO 6	Comprehend advanced Embedded Controllers, Features and case studies

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Micro project/Course based project: 20 marks
Course based task/Seminar/Quiz: 10 marks
Test paper, 1 no. : 10 marks
The project shall be done individually. Group projects not permitted. Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the University. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks. Total duration of the examination will be 150 minutes.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **221TEC001**	***Course Name:*** **SYSTEM DESIGN USING EMBEDDED PROCESSORS**	
Time : 2.5 Hours	Maximum : 60 Marks	
PART A (Answer all questions)		
1	How do we classify the embedded systems based on complexity of applications? Detail each category with examples.	5 marks
2	Discuss the Interconnect Matrix concepts in ARM Cortex M4 Microcontroller	5 marks
3	Discuss the usage of the Watchdog timer with suitable examples.	5 marks
4	Discuss how to enable Advanced Encryption Standard (AES) based applications using ARM Cortex M4.	5 marks
5	Write a short note on programming for Power-Efficient Computing techniques.	5 marks
PART B (Answer any 5 questions)		
6.	Compare and contrast ARM, Thumb, and Thumb-2 instruction set architecture in ARM processors.	7 marks
7	Discuss the AMBA and AXI bus.	7 marks
8.	With help of a block diagram explain the architecture of ARM Cortex M4 Microcontroller.	7 marks
9.	Explain the working of NVIC on ARM Cortex M4.	7 marks
10.	Write down the steps required to implement an application with the following events in embedded C on Cortex M4 Microcontroller. Assume that initially both LEDs are OFF and Blue & Green LEDs are connected to Ports PB6 and PB7 respectively. i. Receive a character send from PC through USART2. ii. Switch ON the Green LED once character 'A' is	7 marks

	received iii. Switch OFF Green LED on receiving 'B'. iv. Switch ON Blue LED the once character 'C' is received Switch OFF Blue LED on receiving 'D'.	
11.	Write a short note on i. Quad SPI in ARM cortex M4 ii. Memory protections	7 marks
12.	Design a real-time data acquisition system using ARM Cortex M4 Microcontroller. It is required to periodically monitor and control the temperature in a boiler which ranges from 0°C to 140°C. The temperature has to be kept at a set-point of 60°C ± 5°C. Provision should be given for receiving the set-point value of temperature from the PC. Illustrate the design with appropriate block diagrams and flowcharts.	7 marks

Syllabus

Module1: Introduction to Embedded Systems

Overview of embedded system architecture, Development and debugging Tools for Embedded Systems,Overview ARM Architecture - Architecture Versions, Instruction Set Development,Thumb-2 and Instruction Set Architecture,AMBA, AXI bus overview.Overview of the Arm Cortex-Mx Processor Architectures.

Module2: ARM Cortex M4 Microcontroller system

ARM Cortex M4 Core, Interconnect Matrix in ARM Cortex M4 Microcontroller,System configuration Controller, NVIC, External Interrupt Controllers, DMA,Reset and Clock Control, Clock Recovery System, Power Control.

Module3: ARM Cortex M4 Microcontroller Peripheral Overview

ARM Cortex M4 Core, Interconnect Matrix in ARM Cortex M4 Microcontroller,System configuration Controller, NVIC, External Interrupt Controllers, DMA,Reset and Clock Control, Clock Recovery System, Power Control.

Module4: Memory, Safety and Security in ARM Cortex Microcontroller

Flash, Quad SPI Interface, Flexible Memory controller,CRC, Random Number Generator, memory protections,Advanced Encryption Standard HW Accelerator (AES), Safety support.

Module5: Advanced Embedded Controllers, Features and case studies

Programming for Power-Efficient Computing - High Level and low level Techniques,Cortex M7, M23 and M33 Controllers and Features,Overview of mbed platform,Embedded Systems case studies - Consumer, Medical, Automotive.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in the third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Introduction to Embedded Systems**	
1.1	Overview of embedded system architecture,	**1**
1.2	Development and debugging Tools for Embedded Systems	**1**
1.3	Overview ARM Architecture - Architecture Versions, Instruction Set Development, Thumb-2 and Instruction Set Architecture,	**3**
1.4	AMBA,AXI bus overview.	**2**
1.5	Overview of the Arm Cortex-Mx Processor Architectures	**2**
2	**ARM Cortex M4 Microcontroller system**	
2.1	ARM Cortex M4 Core, Interconnect Matrix in ARM Cortex M4 Microcontroller	**3**
2.2	System configuration Controller, NVIC, External Interrupt Controllers, DMA	**3**
2.3	Reset and Clock Control, Clock Recovery System, Power Control	**2**
3	**ARM Cortex M4 Microcontroller Peripheral Overview**	
3.1	Introduction to Arm Cortex-M4 Programming, overview of CMSIS	**1**
3.2	GPIO, ADC, DAC	**3**
3.3	Communication & Peripherals - USART, UART, I2C, SPI, USB, CAN	**3**
3.4	Watchdogs and Timers, PWM	**3**
4	**Memory, Safety and Security in ARM Cortex Microcontroller**	
4.1	Flash, Quad SPI Interface, Flexible Memory controller	**3**
4.2	CRC, Random Number Generator, memory protections	**3**
4.3	Advanced Encryption Standard HW Accelerator (AES), Safety support	**2**
5	**Advanced Embedded Controllers, Features and case studies**	
5.1	Programming for Power-Efficient Computing - High Level and low level Techniques	**2**
5.2	Cortex M7, M23 and M33 Controllers and Features	**1**
5.3	Overview of mbed platform	**1**
5.4	Embedded Systems case studies - Consumer, Medical, Automotive	**2**

Text Books

1. Yiu J. The Definitive Guide to ARM Cortex M3 and Cortex M4 Processors, 3rd Edition, Elsevier
2. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier.

Reference Books

1. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education
2. Cortex-M4 Technical Reference Manual (TRM)
3. Raj Kamal, “Microcontroller - Architecture Programming Interfacing and System Design” 1st Edition, Pearson Education
4. P.S Manoharan, P.S. Kannan, “Microcontroller based System Design”, 1st Edition, Scitech Publications

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221TEC012	ELECTRONIC SYSTEM DESIGN	Program Core	3	0	0	3

Preamble:

The objective of this course is to make students understand, practice Design process Protection requirement and to make them capable of independently designing complex systems. The main thrust of Electronic System Design is addressing ways to "tame" the physical effects and control the unwanted side effects of the large-scale integration. The objective is to make the system reliable in production and use, and to make it resilient against external influences.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn Design Process and Its Fundamentals Attain comprehensive understanding of Design Process and its fundamentals. (Cognitive knowledge level: Understand)
CO 2	Attain comprehensive understanding of System Architecture and Protection Requirements (Cognitive knowledge level: Understand).
CO 3	Attain understanding in Reliability Analysis (Cognitive knowledge levels: Understand, analyse, &create).
CO 4	Attain understanding in designing and analysing Thermal Management and Cooling of electronic product (Cognitive knowledge levels: Understand, analyse, and create). Learn how Thermal Management and Cooling is done
CO 5	Enable design of Product that meets the requirement of Electromagnetic Compatibility (EMC) (Cognitive knowledge levels: Understand, analyse, create & Evaluate).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	-	-	-	-
CO 2	-	3	-	-	-
CO 3	2	-	-	-	3
CO 4	-	3	3	3	-
CO 5	-	-	-	-	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : **15 marks**

Course based task/Seminar/Data collection and interpretation: **15 marks**

Test paper, 1 number: **10 marks**

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the University. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks. Total duration of examination will be 150 minutes.

Model Question paper

U	Slot **[SLOT]**
Reg. No:	Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION

Subject: 221EEC006	***ELECTRONIC SYSTEM DESIGN***
Time : 2Hr 30 minute	**Maximum : 60 Marks**

	PART A (Answer all questions)	
1	With proper depiction illustrate the Electronic System Design Process for a Mobile Phone	5 marks
2.	With a suitable example detail the techniques to avoid Electronic component Failure	5 marks
3.	What are thermal management products?	5 marks
4.	Detail the techniques to avoid noise generation and coupling mechanisms in electronic systems	5 marks
5	Describe in detail the product recycling and its advantages.	5 marks
	PART B (Answer any five questions)	
6.	Prepare a feasibility study report involved during product planning.	7 marks
7.	Suppose 10 devices are tested for 500 hours. During the test 2 failures occur. Estimate of the MTBF and failure rate.	7 marks
8.	What are the most common electronic components that fail? Detail the various protection schemes.	7 marks
9.	Select a Heat Sink for TO-220 package outline device is dissipating 7 watts (Q), The Maximum Junction Temperature, is Tj = 125°C, and the Maximum Ambient Temperature, is Ta = 65°C, Component Junction-to-Case Thermal Resistance, is Rθjc = 2.5 °C/W, Assuming that: • Interface material is Silicon Grease – Wakefield 120 Series • 0.002 inches thick • 0.36 in2 contact area The Thermal Resistance of Silicon Oil-Based Grease can be	7 marks

	found to be as: Thermal Resistivity, (ρ), (120 Series = 56 C-in/W), thickness, (t), (in) and contact area, (A), (in^2)	
10.	With proper depiction illustrate the thermal management in electronic circuitry?	7 marks
11.	Analyze various aspects of noise coupling and power integrity in integrated circuits?	7 marks
12.	What are the 5 steps of the recycling process? Illustrate the recycling process with an example.	7 marks

Syllabus

The syllabus address the architecture and fundamental structure of the design process of electronic systems and different ways to "tame" the physical effects and control the unwanted side effects of the large-scale integration, the heat that is dissipated in the electronic system. How to avoid products malfunction because of electromagnetic interference.

Module I: Design Process and Its Fundamentals

Life Cycle of Electronic Products, Design and Development Process, Guidance for Product Planning, Design and Development, Technical Drawings, Circuit Diagrams, Computer-Aided Design (CAD), System Architecture and Protection Requirements, System Design Architecture, Electronic System Levels, System Protection.

Module II: Reliability Analysis

Calculation Principles, Exponential Distribution, Failure of Electronic Components, Failure of Electronic Systems, Reliability Analysis of Electronic Systems, Recommendations for Improving Reliability of Electronic Systems

Module III: Thermal Management and Cooling

Introduction—Terminology, Temperatures, and Power Dissipation, Calculation Principles, Heat Transfer, Methods to Increase Heat Transfer, Application Examples in Electronic Systems, Recommendations for Thermal Management of Electronic Systems

Module IV: Electromagnetic Compatibility (EMC)

Coupling Between System Components, Grounding Electronic Systems, Shielding from Fields, Electrostatic Discharge (ESD), Recommendations for EMC - Compliant Systems Design

Module V: Recycling Requirements and Design for Environmental Compliance

Introduction—Motivation and the Circular Economy, Design and Development for Disassembly, Material Suitability in Design and Development, Recommendations for Environmentally Compliant Systems.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module I - Design Process and Its Fundamentals**	
1.1	Design & Development process	**3**
1.2	System Architecture and Protection Requirements	**3**
1.3	System Protection	**2**
2	**Module II - Reliability Analysis**	
2.1	Failure of Electronic Components	**3**
2.2	Failure of Electronic Systems	**3**
2.3	Reliability Analysis of Electronic Systems	**2**
3	**Module III - Thermal Management and Cooling**	
3.1	Terminology, Temperatures, and Power Dissipation	**3**
3.2	Heat Transfer	**3**
3.3	Enclosure	**2**
4	**Module IV - Electromagnetic Compatibility (EMC)**	
4.1	Coupling Between System Components	**2**
4.2	Electrostatic Discharge (ESD)	**2**
4.3	Grounding Electronic Systems	**2**
4.4	Shielding from Fields	**2**
5	**Module V - Recycling Requirements and Design for Environmental Compliance**	
5.1	Product Recycling in the Disposal Process	**3**
5.2	Design and Development for Disassembly	**3**
5.3	Material Suitability in Design and Development	**2**

Text Books

1. Fundamentals of Electronic Systems Design Jens Lienig, Hans Brümmer Springer Cham Publishers
2. Birolini, Reliability Engineering. Theory and Practice, 7th edition, Springer, 2014
3. R. Reemsburg, Thermal Design of Electronic Equipment (Electronics Handbook), CRC Press, 2000
4. Tecknit, Electromagnetic Compatibility Guide, 1998

Reference Books

1. A practical guide to EMC Engineering Levent Sevgi Artech House Publishers
2. The Electrical Engineering Handbook Series Richard C Dorf CRC Press
3. Designing Electronic Product Enclosures Tony Serksnis Springer Cham Publishers

4. Fundamentals of Electronic Circuit Design Hongshen Ma Wiley; 1st edition (May 21, 2002)
5. Recycling for Climate Protection, Report of the Fraunhofer Institute for Environmental, Safety, and Energy Technology UMSICHT, February 8, 2011. Online at:http://www.alba.info/fileadmin/alba/pressemappe/recycling_fuer_den_klimaschutz/110210_CO2_Studie_ALBA_Group_final_v4.pdf

PROGRAM ELECTIVE I

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC063	EMBEDDED PROGRAMMING	PROGRAM ELECTIVE 1	3	0	0	3

Preamble: The C Standards Committee created the Embedded C as a collection of language extensions for the C programming language to address commonality concerns that emerge with C extensions for various embedded systems. It's used to create microcontroller programming software Fixed-point arithmetic, named address spaces, and essential I/O hardware addressing are all characteristics not accessible in normal C. The course also covers object oriented programming using C++. The course will give an overview of Coding Standards For Compliance.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of fundamentals of C Programming (Cognitive knowledge level: **Understand**).
CO 2	Attain comprehensive understanding of Embedded C (Cognitive knowledge level: **Understand**).
CO 3	Attain comprehensive understanding of Embedded Programming and development Tools (Cognitive knowledge levels: **Understand, analyse, &create**)
CO 4	Attain comprehensive understanding of fundamentals of Comprehend the fundamentals of C++ (Cognitive knowledge levels: **Understand, analyse, &create**)
CO 5	Attain comprehensive understanding of the state-of- art hardware and software tools for Embedded software development (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Attain comprehensive understanding of the Embedded Programming Coding standards & Concepts (Cognitive knowledge levels: **Understand & Apply**)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

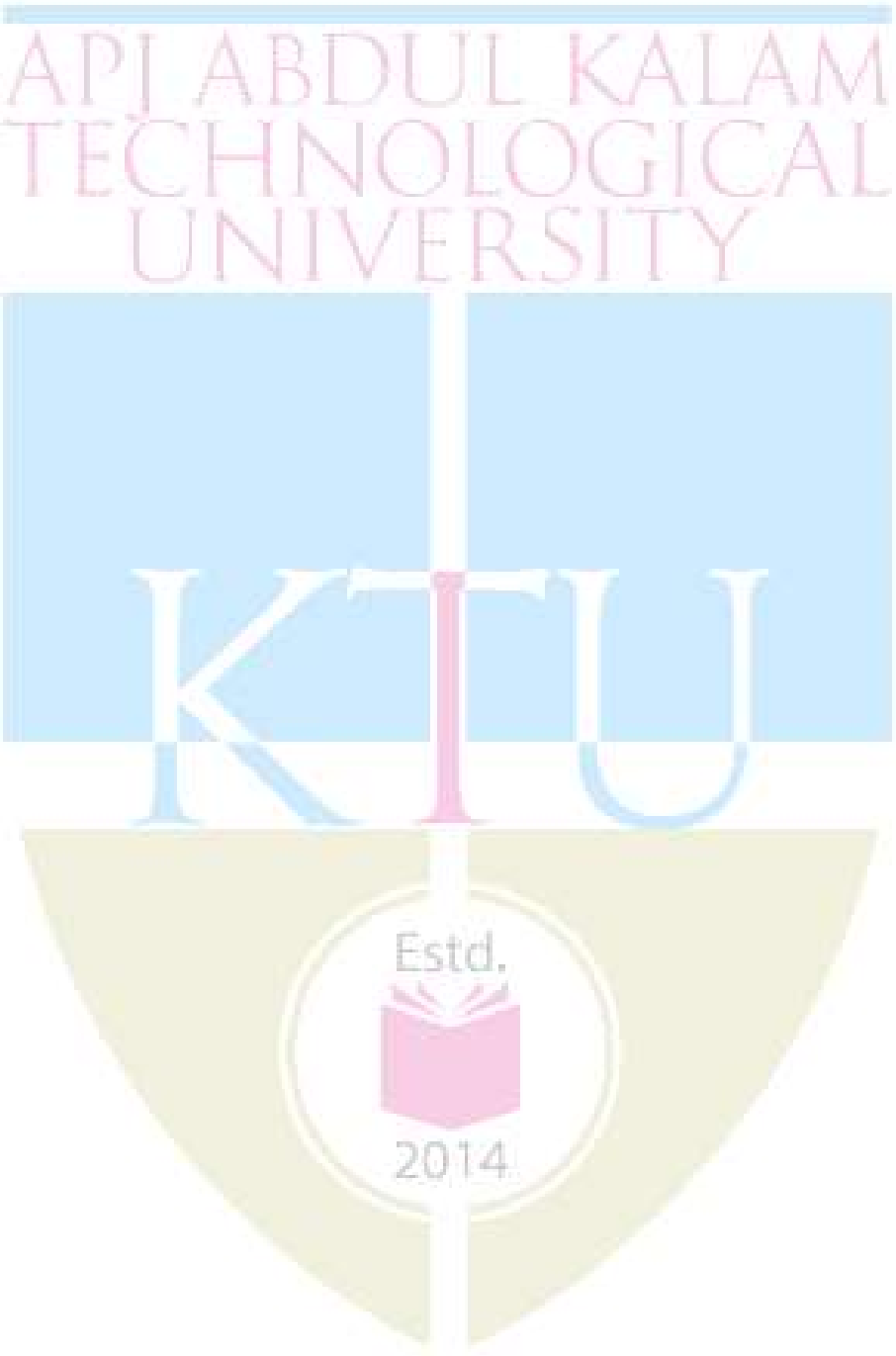
Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in

the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.



Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **221TEC002**	***Course Name:*** **Embedded Programming**	
Time : 2.5 Hours	Maximum : 60 Marks	
PART A (Answer all questions)		Marks
1	Discuss about types of UML modeling.	5
2	What is Makefile? Discuss its usage with suitable examples.	5
3	Illustrate the difference between C and Embedded C.	5
4	Briefly explain the polymorphism concepts with suitable examples.	5
5	Explain the MISRA C standard and its relevance in Embedded software development.	5
PART B (Answer any five questions)		Marks
6.	What do you mean by algorithm? Also write the algorithm to find multiplication of two matrices.	7
7.	Write a short note on i. GNU profiler ii. GNU C Compiler and compiler options	7
8.	Write a C program to implement singly linked list	7
9.	Explain function overloading with the help of a suitable C++ program.	7
10	Describe inheritance concepts with suitable C++ programs.	7
11	Discuss the compute bound optimisation techniques in detail.	7
12	Describe IEEE-754 standard and applications.	7

Syllabus

Module1: Introduction to Programming & algorithms for problem solving

The Basic Model of Computation, Algorithms, Flow-charts, Programming Languages, Compilation, Linking and Loading, Testing and Debugging, Algorithms for Problem Solving:Decimal Base to Binary Base conversion, Reversing digits of an integer, GCD (Greatest Common Division), LCM etc. , Use case diagrams and UML.

Module2: C Programming Basics

GNU Tools: gcc, gdb, gprof, Makefiles, Basic data types, operations, and flow control (decision-making statements), Flow control (loops), typecasting, and computer logic, Switch-case, arrays, and the basics of strings, pointers, functions, storage class.

Module3: Advanced C programming for Embedded Systems

Structure and union, Linear and nonlinear data structures, Linked List.

Module4: Object Oriented Programming concepts with C++

Overview of C++, Fundamentals of the object-oriented approach, Class hierarchy, Advanced class concepts, Templates, Accessing data and dealing with exceptions.

Module5: Embedded Programming Coding standards & Concepts

Coding Standards For Compliance , ANSI C, C89, C95, C99, C11, MISRA C & C++, Profiling & Optimisation techniques, Pragma , floating-point exceptions rounding multi-precision libraries (GMP, MPFR, MPIR), IEEE-754, Static and dynamic Code analysis.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in the third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module1**: Introduction to Programming & algorithms for problem solving	
1.1	The Basic Model of Computation	1
1.2	Algorithms, Flow-charts, Programming Languages, Compilation, Linking and Loading, Testing and Debugging	1
1.3	Algorithms for Problem Solving:Decimal Base to Binary Base conversion, Reversing digits of an integer, GCD (Greatest Common Division), LCM etc.	3
1.4	Use case diagrams and UML	2
2	**Module2**:C Programming Basics	
2.1	GNU Tools: gcc, gdb, gprof, Makefiles	2
2.2	Basic data types, operations, and flow control (decision-making statements), Flow control (loops), typecasting, and computer logic, Switch-case, arrays, and the basics of strings.	3
2.3	pointers, functions, storage class	3
3	**Module3**:Advanced C programming for Embedded Systems	
3.1	Structure and union	3
3.2	Linear and nonlinear data structures	1
3.3	Linked List	2
4	**Module4**: Object Oriented Programming concepts with C++	
4.1	Overview of C++, Fundamentals of the object-oriented approach	3
4.2	Class hierarchy, Advanced class concepts	4
4.3	Templates, Accessing data and dealing with exceptions	2
5	**Module5**: Embedded Programming Coding standards & Concepts	
5.1	Coding Standards For Compliance , ANSI C, C89, C95, C99, C11, MISRA C & C++	2
5.2	Profiling & Optimisation techniques	2
5.3	Pragma , floating-point exceptions rounding multi-precision libraries (GMP, MPFR, MPIR)	2
5.4	IEEE-754	1
5.5	Static and dynamic Code analysis	1

Text Books

1. C Programming language, Kernighan, Brian W, Ritchie, Dennis M, Prentice Hall PTR
2. “Embedded C”,Michael J. Pont, Addison Wesley

Reference Books

1. The Complete Reference C++, Herbert Schildt, TMH
2. GNU C++ For Linux, Tom Swan , Prentice Hall India
3. Daniel W. Lewis, “Fundamentals of embedded software where C and assembly meet”, Pearson Education, 2002.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC100	ADVANCED DIGITAL SYSTEM DESIGN	PROGRAM ELECTIVE 1	3	0	0	3

Preamble:

The objective of this course is to make students understand, practice and apply digital design principles and insights, to make them capable of independently designing complex digital systems.

The course covers various facets of digital system design and focuses on designing from the scratch. The course focuses on designing combinational and sequential building blocks, using these building blocks to design complex digital systems

Course Outcomes:

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of computer arithmetic fundamentals. (Cognitive knowledge level: **Understand**).
CO 2	Attain comprehensive understanding of digital design fundamentals (Cognitive knowledge level: **Understand**).
CO 3	Attain understanding in designing and analysing combinational circuit and subsystems (Cognitive knowledge levels: **Understand, analyse, &create)**.
CO 4	Attain understanding in designing and analysing sequential circuit and subsystems (Cognitive knowledge levels: **Understand, analyse, & create).**
CO 5	Enable design of data path units and control units for microcomputer designs (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Understand digital logic testing methods for reliability and their applications. Cognitive knowledge levels: **Understand & Apply**).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1			2			
CO 2			2		3		
CO 3		1	2		3	2	
CO 4	3		2		3	2	
CO 5			2			3	

CO 6			2			2	

Assessment Pattern

Bloom's Category	**End Semester Examination**
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2.5 hours

Continuous Internal Evaluation: 40 marks
Preparing a review article based on peer reviewed
Original publications (minimum 10publications shall be referred):15marks
Course based task/Seminar/Data collection and interpretation: 15marks
Test paper, 1 no. : 10 marks
Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

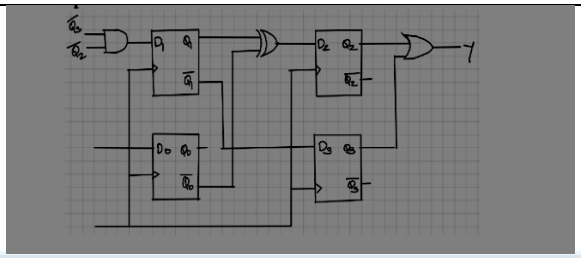
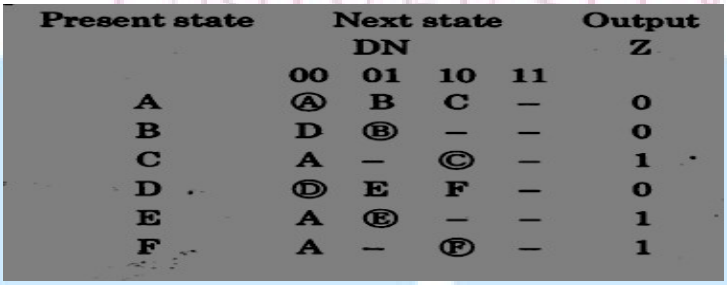
Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

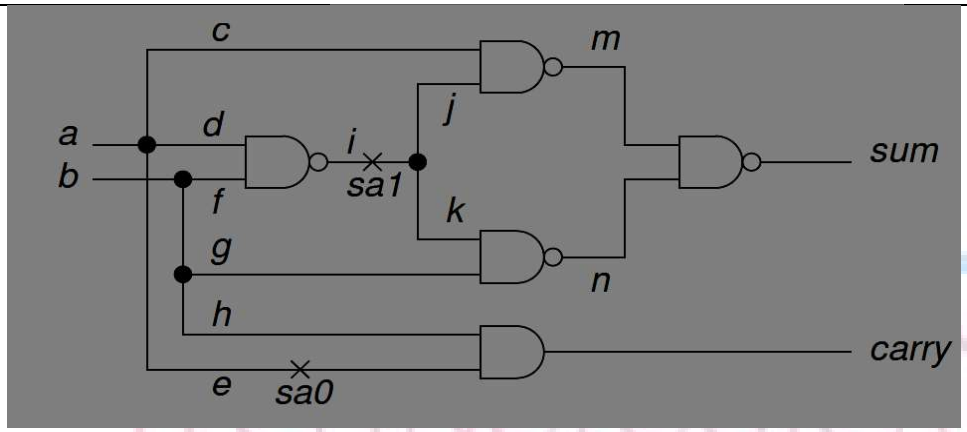
Course Name: ADVANCED DIGITAL SYSTEM DESIGN

Maximum : 60 Marks

<table>
<tr><td colspan="2">PART A (Answer all questions)</td><td></td></tr>
<tr><td>1</td><td>Find out the status of carry, overflow and sign flags of a processor’s program status word (PSW) after performing the addition of the following 2’s complement numbers :01001101 and 11101001</td><td>5 marks</td></tr>
<tr><td>2.</td><td>Implement the following truth table using Multiplexers.
<table>
<tr><td>S1 S0</td><td>Y3 Y2 Y1 Y0</td></tr>
<tr><td>0 0</td><td>D3 D2 D1 D0</td></tr>
<tr><td>0 1</td><td>D0 D3 D2 D1</td></tr>
<tr><td>1 0</td><td>D1 D0 D3 D2</td></tr>
<tr><td>1 1</td><td>D2 D1 D0 D3</td></tr>
</table></td><td>5 marks</td></tr>
<tr><td>3.</td><td>Design a circuit to convert RS Flip-flop into JK Flip-flop.</td><td>5 marks</td></tr>
<tr><td>4.</td><td>Design a 3-bit Mod-5 self-correcting binary counter.</td><td>5 marks</td></tr>
<tr><td>5</td><td>Explain Boolean difference method of test pattern generation with an example.</td><td>5 marks</td></tr>
<tr><td colspan="2">PART B (Answer any five questions)</td><td></td></tr>
<tr><td>6.</td><td>Design a sequential network to convert BCD to Excess-3 code.The input and output will be serial with the least significant bit first.</td><td>7 marks</td></tr>
<tr><td>7.</td><td>Convert the given number in IEEE754 Double precision format as well as in POSIT format.</td><td>7 marks</td></tr>
<tr><td>8.</td><td>Find the critical path and maximum frequency of operation of the following circuit. Given: t setup =t_{hold}=4ns, t_{pd}=6ns and t_{gate}=5ns.</td><td>7 marks</td></tr>
</table>

		
9.	Given below is the initial flow table of a simple 'vending machine'. Analyze the merging procedures and arrive at the reduced flow table through the primitive flow table. 	7 marks
10.	Design a sequential Traffic light controller using Moore Graph for the intersection of street "P" and street "Q". Each street has traffic sensors, which detect the presence of vehicles approaching or stopped at the intersection. S_P=1 indicates vehicle approaching on "P" and S_Q= 1 for "Q". Street P is the main street and has a Green light until a vehicle approaches on "Q". Then light changes and "Q" has green light. At the end of 50 seconds the light changes back unless there is a vehicle on street "Q" and none on "P". Then "Q" gets extended time of 10 s. Let there are three outputs G_P Y_P R_P for street "P' and three outputs G_Q Y_Q R_Q for street "Q".	7 marks
11.	Design a sequence detector circuit to detect 1010 with overlapping.	7 marks
12.	Consider the circuit shown below ; How many test vectors are there that detects both the faults, i) ***sa1*** and ii) ***sa0?*** _____ Perform Parallel Fault simulation for the input test vector (a, b)=(1,1) and comment on the result ____	7 marks

Present state	Next state DN				Output Z
	00	01	10	11	
A	Ⓐ	B	C	—	0
B	D	Ⓑ	—	—	0
C	A	—	Ⓒ	—	1
D	Ⓓ	E	F	—	0
E	A	Ⓔ	—	—	1
F	A	—	Ⓕ	—	1


c
m
a
d
i
j
sum
b
sa1
f
k
g
n
h
carry
e
sa0

Syllabus

MODULE 1: PROCESSOR ARITHMETIC

Two's Complement Number System – Arithmetic Operations,Floating Point Number system – IEEE 754 format & POSIT, Basic binary codes.

MODULE 2: COMBINATIONAL LOGIC DESIGN

Functional blocks – Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators, Adders, substractor, carry look- ahead adder, timing analysis. Combinational multiplier structures, Timing hazards.

MODULE 3: SEQUENTIAL LOGIC DESIGN

Latches and Flip-Flops, Sequential logic circuits – timing analysis (Set up and hold times) Synchronizers and met stability,State machines – Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning;FSM Design examples: Vending machine, Traffic light controller, Washing machine.

MODULE 4: DIGITAL SUBSYSTEMS

ALU, 4-bit combinational multiplier, Barrel shifter,Simple fixed point to floating point encoder, Dual Priority encoder, Cascading comparators .Pattern (sequence) detector, Programmable Up-down counter, Round robin arbiter with 3 requesters, Process Controller, FIFO

MODULE 5: DIGITAL LOGIC TESTING

Introduction to digital logic testing,Fault modelling, fault collapsing, fault simulation, test generation,Introduction to Design For Testability(DFT),DFT and Built-In-Self-Test(BIST)

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**MODULE 1: PROCESSOR ARITHMETIC:**	
1.1	Two's Complement Number System – Arithmetic Operations	**1**
1.2	Floating Point Number system – IEEE 754 format & POSIT	**3**
1.3	Basic binary codes.	**3**
2	**MODULE 2: COMBINATIONAL LOGIC DESIGN**	
2.1	Functional blocks – Decoders, Encoders, Three-state devices, Multiplexers, Parity circuits, Comparators,	**3**
2.2	Adders, subtractors, carry look- ahead adder, timing analysis. Combinational multiplier structures.	**4**
2.3	Timing hazards	**1**
3	**MODULE 3: SEQUENTIAL LOGIC DESIGN**	
3.1	Latches and Flip-Flops, Sequential logic circuits – timing analysis (Set up and hold times) Synchronizers and met stability.	**2**
3.2	State machines – Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning;	**4**
3.3	FSM Design examples: Vending machine, Traffic light controller, Washing machine.	**2**
4	**MODULE 4: DIGITAL SUBSYSTEMS**	
4.1	ALU, 4-bit combinational multiplier, Barrel shifter,	**2**
4.2	Simple fixed point to floating point encoder, Dual Priority encoder, Cascading comparators.	**2**
4.3	Pattern (sequence) detector, Programmable Up-down counter, Round robin arbiter with 3 requesters Process Controller, FIFO	**4**
5	**MODULE 5: DIGITAL LOGIC TESTING**	
5.1	Introduction to digital logic testing	**2**
5.2	Fault modelling, fault collapsing, fault simulation, test generation	**4**
5.3	Introduction to Design For Testability(DFT),DFT and Built-In-Self-Test(BIST)	**2**

Text Books

1. Digital Design by Frank,John Wiley and Sons Publishers.
2. Digital Computer Arithmetic Datapath Design Using Verilog HDL by James E. Stine, Spinger
3. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. Bushnell ,Vishwani Agrawal,Springer.

Reference Books

1. Digital Design by M. Morris R. Mano and Michael D. Ciletti.,Pearson Education.
2. Gustafson and Yonemoto. 2017. Beating Floating Point at its Own Game: Posit Arithmetic. Supercomputing Frontiers and Innovations: an International Journal, Volume 4I, ssue 2, June 2017 , pp 71–86, https://doi.org/10.14529/jsfi170206.
3. Digital Design Principles and Practices by John F. Wakerly, Pearson Education.
4. An Introduction to Logic Circuit Testing by Parag K. Lala, Morgan & Claypool Publishers.
5. Digital Systems Testing and Testable Design by Melvin A. Breuer , Arthur D. Friedman, MironAbramovici, Wiley-IEEE Press

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC107	ELECTRONIC PACKAGING	PROGRAM ELECTIVE 1	3	0	0	3

Preamble:

The objective of this course is to take the students to the multidisciplinary area of electronics systems packaging critically significant in product design. Learn the role of Packaging as IC and Device Packaging, and Microsystems Packaging, Systems Packaging to go from wafer to complete system. Learn the role of electrical, mechanical and materials in Systems Packaging

Course Outcomes:

After the completion of the course the student will be able to

CO 1	Learn the packaging in microelectronics, IC Packaging, IC Packaging Challenges (Cognitive knowledge level: Understand)
CO 2	Attain comprehensive understanding of Electrical Anatomy of Systems Packaging (Cognitive knowledge level: Understand).
CO 3	Design using Single Chip and Multi Chip Packages (Cognitive knowledge levels: Understand, analyse, &create)
CO 4	Learn different ways of Printed Wiring Board Fabrication (Cognitive knowledge levels: Understand, analyse, create).
CO 5	Design System-Level Electrical Testing (Cognitive knowledge levels: Understand, analyse, create & Evaluate).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	-	-	-	-
CO 2	-	3	-	-	-
CO 3	2	-	-	-	3
CO 4	-	3	3	3	-
CO 5	-	-	-	-	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30

Create	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern:

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : **15 marks**

Course based task/Seminar/Data collection and interpretation: **15 marks**

Test paper, 1 number : **10 marks**.
Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

U	Slot **[SLOT]**
Reg. No:	Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

FIRST SEMESTER M.TECH DEGREE EXAMINATION

Subject: 221EEC107	**ELECTRONIC PACKAGING**
Time : 2Hr 30 minute	Maximum : 60 Marks

	PART A (Answer all questions)	
1	With proper depiction briefly describe IC and System Packaging?	5 marks
2.	Derive the equation for the maximum effective inductance L_{eff} that can be tolerated on the power distribution	5 marks
3.	As a design engineer, list possible requirements with explanation, for a SCP to be used in any three of the following applications: a) hand held video game, b) cell phone, c) personal digital assistant, d) laptop computer, e) cable set top box, f) desktop PC, g) high-end workstation, h) supercomputer, i) hearing aid, j) implantable pacemaker	5 marks
4.	Why is packaging very important for RF applications?	5 marks
5	Discuss Anatomy for system-level Electrical Testing	5 marks
	PART B (Answer any five questions)	
6.	How Systems Packaging Involves Electrical, Mechanical and Materials Technologies	7 marks
7.	Construct an RC circuit to represent an interconnection with R = 100. The capacitance of the capacitor varies from 1pF to 5pF in steps of 1pF. Using a pulse as the input, calculate the 50% delay produced by the circuit. The response is equivalent to that of a CMOS inverter charging a capacitive load	7 marks
8.	A trace with length 4 cm is routed through a polyimide substrate. a) Determine the transit time delay associated with this interconnect. b) If the system in question has parameters Ron= 50Ω and Cg = 2 pF, does the capacitive	7 marks

<table>
<tr><td></td><td>gate delay T 50% dominate the delay time, or does the transit time delay?
c) If the trace has width 40 μm and is separated from a solid ground plane by 10 μm,
determine its capacitance per unit length
d) If the total capacitance of the interconnect (obtained from the capacitance per unit length)</td><td></td></tr>
<tr><td>9.</td><td>What are the Functions of Single CHIP Packages</td><td>7 marks</td></tr>
<tr><td>10.</td><td>A typical central office system environment will have a maximum ambient temperature of 35°C. The corresponding rise in internal ambient for a desktop system used in this environment should be no greater than 10°C above the external ambient. A processor chip used in such a system is packaged in a thermally enhanced 560-pin plastic BGA, also known as Super BGA, with the thermal conductivity properties listed in Table If the maximum power dissipated by the processor is 8.0 watts, determine the range of air flow velocities needed to limit the chip junction temperature to a) 85°C, b) 100°C, and, c) 125°C. What is the package case temperature in each of these situations?
<table>
<tr><th>Material</th><th>Dielectric Constant</th><th>Elastic Modulus (Gpa)</th><th>Tensile Strength (Mpa)</th><th>Thermal Conduct. (W/m K at 20°C)</th><th>Coeff. Thermal Expansion (ppm/°C)</th><th>Electrical Resistivity (ohm-cm)</th></tr>
<tr><td>Substrate, case, thermal interface</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Alumina (92%)</td><td>7.9–10.0</td><td>55</td><td>157</td><td>18</td><td>6.8</td><td>10E14</td></tr>
<tr><td>Laminate (BT)</td><td>4.0</td><td>12–18</td><td>225–300</td><td>—</td><td>15–20</td><td>—</td></tr>
<tr><td>Cu</td><td>NA</td><td>125</td><td>270</td><td>—</td><td>16</td><td><2E-6</td></tr>
<tr><td>Cu-W (90%)</td><td>NA</td><td>255</td><td>—</td><td>180–200</td><td>6.5</td><td><6E-6</td></tr>
<tr><td>Molding compound</td><td>≦5.0</td><td>11.7</td><td>20</td><td>0.6</td><td>23</td><td>5E12</td></tr>
<tr><td>Leads/pins, leadframe</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Kovar</td><td>NA</td><td>138</td><td>627</td><td>17.5</td><td>5.3</td><td>49E-6</td></tr>
<tr><td>Alloy 42</td><td>NA</td><td>145</td><td>588–735</td><td>15.7</td><td>4.5</td><td>57E-6</td></tr>
<tr><td>Solder spheres (BGA)</td><td>NA</td><td>30</td><td>35</td><td>51</td><td>25</td><td>—</td></tr>
<tr><td>Die attach</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>Ag filled epoxy</td><td>—</td><td>—</td><td>—</td><td>1.6</td><td>46</td><td>2E-4</td></tr>
<tr><td>Encapsulant</td><td>3.8</td><td>5–13</td><td>70</td><td>0.5–0.9</td><td>16–31</td><td>2E16</td></tr>
<tr><td>Solder (tin-lead)</td><td>NA</td><td>30</td><td>35</td><td>50.6</td><td>24.7</td><td>—</td></tr>
</table>
</td><td>7 marks</td></tr>
<tr><td>11.</td><td>Why is SOC application very challenging for 3G systems?</td><td>7 marks</td></tr>
<tr><td>12.</td><td>How does energy consumption throughout the life cycle of electronic products negatively influence the environment?</td><td>7 marks</td></tr>
</table>

Syllabus

Module I - Electronic Systems Packaging - Introduction to microsystems packaging, Microsystem Technologies, System-Level Microsystems Technologies, The role of packaging in microelectronics, IC Packaging, IC Packaging Challenges, The role of packaging in microsystems, What Is the Role of Packaging in the Computer Industry, What Is the Role of Packaging in the Telecommunication Industry, What Is the Role of Packaging in Automotive Systems, What Is the Role of Packaging in Medical Electronics, What Is the Role of Packaging in Consumer Electronics

Module II - Semiconductor Packaging - Fundamentals of electrical package design, Electrical Anatomy of Systems Packaging, Signal Distribution, Power Distribution, Design Process, Fundamentals of design for reliability, Microsystems Failures and Failure Mechanisms, Fundamentals of Design for Reliability, Electrically-Induced Failures, Chemically-Induced Failures, Fundamentals of thermal management, Cooling Requirements for Microsystems, Thermal Management Fundamentals, Thermal Management of IC and PWB Packages, Electronic Cooling Methods

Module III - CHIP Packaging - Functions of Single Chip Packages, Types of Single Chip Packages, Fundamentals of Single Chip Packaging, Materials, Processes, and Properties, Characteristics of Single Chip Packages, Multichip Module Functionality, Multichip Module Advantages, Multichip Modules at the System Level, Types of Multichip Module Substrates, Multichip Module Design, Multichip Module Technology Comparisons, Alternatives to Multichip Modules, Why Wafer-level Packaging?, WLP Technologies, WLP Reliability, Wafer-level Burn-in and Test.

Module IV - Systems Packaging - What Is RF?, RF Applications and Markets, Anatomy of RF Systems, Fundamentals of RF, RF Packaging, RF Measurement Techniques, What Is Encapsulation? What Is Sealing? Why Is Encapsulation Necessary? Fundamentals of Encapsulation and Sealing, Encapsulation Requirements, Encapsulant Materials, Encapsulation Processes, Hermetic Sealing, What Is a System-Level Printed Wiring Board? Types of Printed Wiring Boards, Anatomy of a Printed Wiring Board, Fundamentals of Printed Wiring Boards, Printed Wiring Board Materials, Standard Printed Wiring Board Fabrication, Limitations in Standard Printed Wiring Board Process, Microvia Boards.

Module V - Assembly & Testing - What Is a Printed Wiring Board Assembly? Surface Mount Technology, Through-Hole Assembly, Generic Assembly Issues, Process Control, Design Challenges, What Is Electrical Testing? Why Is Electrical Testing Necessary? Anatomy of System-Level Electrical Testing, Fundamentals of Electrical Tests, Interconnection Tests, Active Circuit Testing, Design for Testability, What Are the Environmental Concerns of Microsystems? How Electronics Production Influences the Environment, Life-Cycle Assessment.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

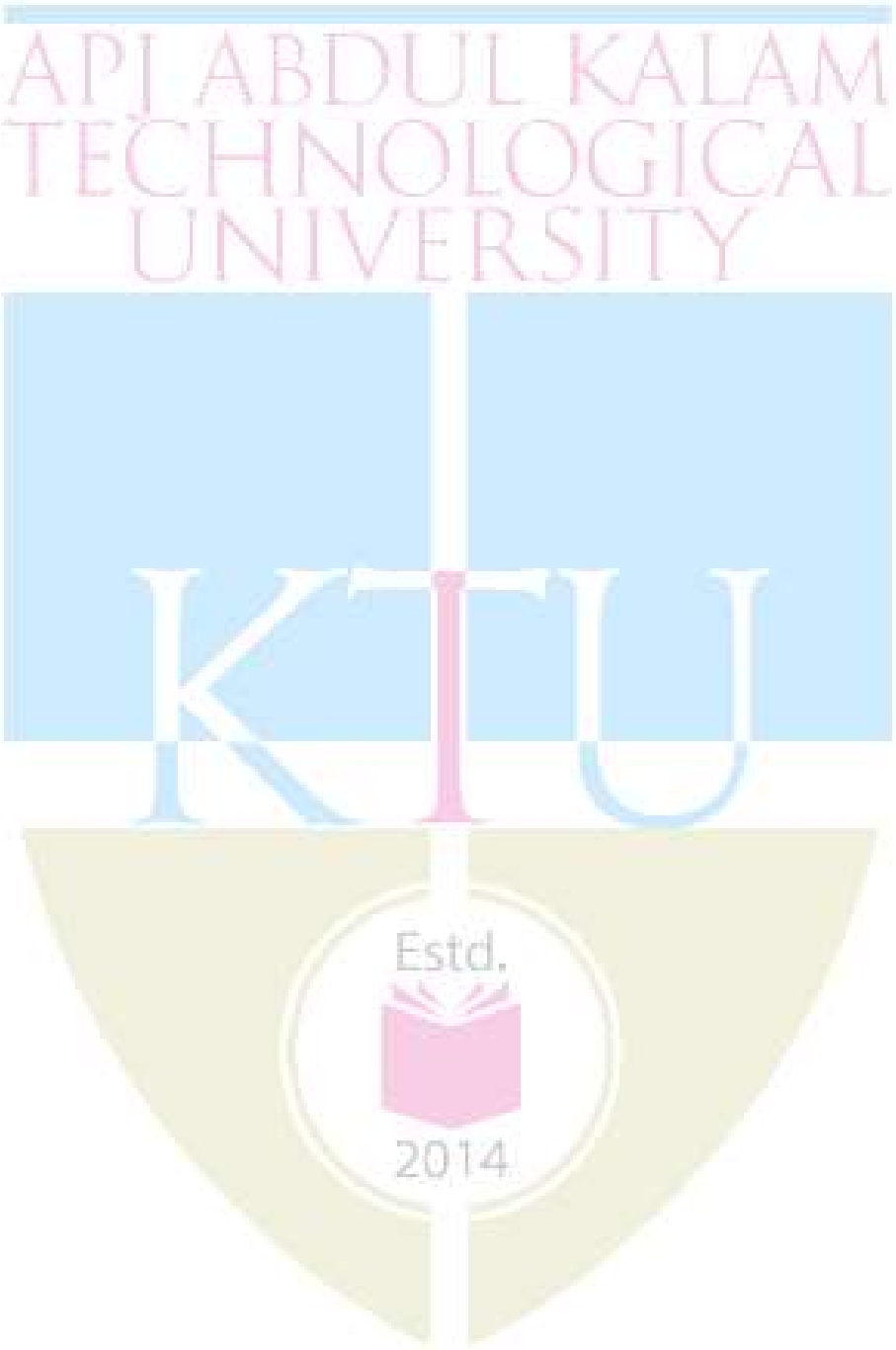
No	Topic	No. of Lectures
1	**ELECTRONIC SYSTEMS PACKAGING**	
1.1	Introduction to microsystems packaging	**3**
1.2	The role of packaging in microelectronics	**3**
1.3	The role of packaging in microsystems	**2**
2	**SEMICONDUCTOR PACKAGING**	
2.1	Fundamentals of electrical package design	**3**
2.2	Fundamentals of design for reliability	**3**
2.3	Fundamentals of thermal management	**2**
3	**CHIP PACKAGING**	
3.1	Fundamentals of single chip packaging	**3**
3.2	Fundamentals of multichip packaging	**3**
3.3	Fundamentals of wafer-level packaging	**2**
4	**SYSTEMS PACKAGING**	
4.1	Fundamentals of RF packaging	**3**
4.2	Fundamentals of sealing and encapsulation	**3**
4.3	Fundamentals of system-level PWB technologies	**2**
5	**ASSEMBLY & TESTING**	
5.1	Fundamentals of board assembly	**3**
5.2	Fundamentals of electrical testing	**3**
5.3	Fundamentals of microsystems design for environment	**2**

Text Books

1. Fundamentals of Microsystems Packaging, Tummala, Rao R., McGraw Hill, 2001
2. Microelectronics packaging handbook, Tummala, Rao R McGraw Hill, 2008

Reference Books

1. Advanced Electronic Packaging, William D. Brown, IEEE Press, 1999
2. The electronic packaging handbook, Blackwell (Ed), CRC Press, 2000



CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC102	CLOUD COMPUTING	PROGRAM ELECTIVE 1	3	0	0	3

Preamble: Cloud computing is an interesting domain, it helps businesses meet their need for software, hardware, and the right type of infrastructure that can keep projects going. Meanwhile, it also offers cost-effective solutions, which would have once cost companies several thousands of dollars. The topic often breaks into sections that focus on the components of a computing cloud, categories of various service types, cloud security, exploring platforms as service, evaluating cloud architectures, etc. These are a few reasons why enrolling in a cloud computing course proves to be useful for professionals.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of the concept of Cloud Computing (Cognitive knowledge level: **Understand**)
CO 2	Attain comprehensive understanding of component level virtualization (Cognitive knowledge level: **Understand**)
CO 3	Attain comprehensive understanding of the Architecture of Cloud Computing (Cognitive knowledge levels: **Understand, analyse, &create**)
CO 4	Attain comprehensive understanding of Parallel and distributed computing (Cognitive knowledge levels: **Understand, analyse, create and apply**)
CO 5	Attain comprehensive understanding of the Cloud Services – IaaS, PaaS, SaaS (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Attain comprehensive understanding of the importance of Cloud Security (Cognitive knowledge levels: **Understand & Apply**)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-

CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	**End Semester Examination**
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: XXXX	***Course Name: Cloud Computing***	
Time : 2.5 Hours		Maximum : 60 Marks
PART A (Answer all questions)		
1.	Write a note on Cloud Services – IaaS, PaaS, SaaS	5 marks
2.	State the differences between a traditional computer and a virtual machine.	5 marks
3.	Explain the design challenges of Cloud Computing Architecture	5 marks
4.	Briefly explain Hadoop Library from Apache	5 marks
5	With proper depiction illustrate why it is harder to establish security in the cloud?	5 marks
PART B (Answer any five questions)		
6.	With proper illustration detail the NIST Cloud Computing Reference Architecture	7 marks
7.	Differentiate Public , Private and Hybrid Clouds	7 marks
8.	Define virtualization. What is the role of VMM in virtualization?	7 marks
9.	Explain various implementation levels of Virtualization.	7 marks
10.	What is the concept of Layered Cloud Architecture Development	7 marks
11.	What is meant by Map Reduce? Explain the logical data flow of MapReduce function using suitable example.	7 marks
12.	Explain Security Architecture Design in cloud.	7 marks

Syllabus

Module1: Introduction to Cloud Computing

Evolution of Cloud Computing, System Models for Distributed and Cloud Computing, NIST Cloud Computing Reference Architecture, Features of Cloud Computing, Cloud Services – IaaS, PaaS, SaaS, Cloud service Providers – Public , Private and Hybrid Clouds.

Module2: Introduction to component virtualization

Basics of Virtualization, Types of Virtualization, Implementation Levels of Virtualization, Virtualization of CPU, Memory, I/O Devices, Desktop Virtualization, Server Virtualization, Storage Virtualization, Network Virtualization.

Module3: Architectural Design of Compute and Storage Clouds

Layered Cloud Architecture Development, Design Challenges, Inter Cloud Resource Management, Resource Provisioning and Platform Deployment, Global Exchange of Cloud Resources.

Module4: Parallel and Distributed Programming Paradigms

Map Reduce, Twister and Iterative MapReduce, Hadoop Library from Apache, Mapping Applications, Programming Support, Google App Engine, Amazon AWS, Cloud Software Environments - Eucalyptus, Open Nebula, OpenStack

Module5: Security Overview

Cloud Security Challenges, Software-as-a-Service Security, Security Governance, Risk Management, Security Monitoring, Security Architecture Design, Data Security, Application Security, Virtual Machine Security.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module1: Introduction to Cloud Computing**	
1.1	Evolution of Cloud Computing	**1**
1.2	System Models for Distributed and Cloud Computing	**1**
1.3	NIST Cloud Computing Reference Architecture	**1**
1.4	Features of Cloud Computing	**1**
1.5	Cloud Services – IaaS, PaaS, SaaS	**1**
1.6	Cloud service Providers – Public , Private and Hybrid Clouds	**1**
2	**Module2: Introduction to component virtualization**	
2.1	Basics of Virtualization	**1**
2.2	Types of Virtualization	**1**
2.3	Implementation Levels of Virtualization	**2**
2.4	Virtualization of CPU, Memory, I/O Devices	**2**
2.5	Desktop Virtualization	**1**
2.6	Server Virtualization	**1**
2.7	Storage Virtualization	**1**
2.8	Network Virtualization	**1**
3	**Module3:Architectural Design of Compute and Storage Clouds**	
3.1	Layered Cloud Architecture Development	**1**
3.2	Design Challenges	**1**
3.3	Inter Cloud Resource Management	**1**
3.4	Resource Provisioning and Platform Deployment	**1**
3.5	Global Exchange of Cloud Resources	**1**
4	**Module4: Parallel and Distributed Programming Paradigms**	
4.1	Map Reduce, Twister and Iterative MapReduce	**1**
4.2	Hadoop Library from Apache	**1**

4.3	Mapping Applications	**1**
4.4	Programming Support	**2**
4.5	Google App Engine	**1**
4.6	Amazon AWS	**1**
4.7	Cloud Software Environments - Eucalyptus, Open Nebula, OpenStack	**3**
5	**Module5: Security Overview**	
5.1	Cloud Security Challenges	**1**
5.2	Software-as-a-Service Security	**1**
5.3	Security Governance	**1**
5.4	Risk Management	**1**
5.5	Security Monitoring	**1**
5.6	Security Architecture Design	**1**
5.7	Data Security, Application Security, Virtual Machine Security	**3**

Text Books

1. Kai Hwang, Geoffrey C Fox, Jack G Dongarra, “Distributed and Cloud Computing, From Parallel Processing to the Internet of Things”, Morgan Kaufmann Publishers, 2012
2. John W.Rittinghouse and James F.Ransome, “Cloud Computing: Implementation, Management, and Security”, CRC Press, 2010

Reference Books

1. Toby Velte, Anthony Velte, Robert Elsenpeter, “Cloud Computing, A Practical Approach”, TMH, 2009
2. George Reese, “Cloud Application Architectures: Building Applications and Infrastructure in the Cloud” O'Reilly, 2009
3. James E. Smith, Ravi Nair, “Virtual Machines: Versatile Platforms for Systems and Processes”, Elsevier/Morgan Kaufmann, 2005
4. Katarina Stanoevska-Slabeva, Thomas Wozniak, Santi Ristol, “Grid and Cloud Computing – A Business Perspective on Technology and Applications”, Springer, 2010

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC103	ELECTRONIC DESIGN AUTOMATION	PROGRAM ELECTIVE 1	3	0	0	3

Preamble:

The objective of this course is to make students understand, practice and apply Electronic design automation (EDA) tools used to design integrated circuit. This course assist students start from specification, design, verification, place, route, functional verification, implements and test component.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn Design Methodology (Cognitive knowledge level: Understand)
CO 2	Attain comprehensive understanding of Symbolic Design Entry (Cognitive knowledge level: Understand).
CO 3	Design using Standard Description Languages (Cognitive knowledge levels: Understand, analyse, &create)
CO 4	Learn different ways of Graphical Descriptions, Partitioning, Optimization (Cognitive knowledge levels: Understand, analyse, create).
CO 5	Learn, Simulation Model, Structure of a Digital Simulator (Cognitive knowledge levels: Understand, analyse, create & Evaluate).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	-	-	-	-
CO 2	-	3	-	-	-
CO 3	2	-	-	-	3
CO 4	-	3	3	3	-
CO 5	-	-	-	-	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : **15 marks**

Course based task/Seminar/Data collection and interpretation: **15 marks**

Test paper, 1 number: **10 marks**

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

U	Slot **[SLOT]**
Reg. No:	Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION

Subject: 221EEC003	**ELECTRONIC DESIGN AUTOMATION**	
Time : 2Hr 30 minute		**Maximum : 60 Marks**
	PART A (Answer all questions)	
1.	What does one has to know in order to use EDA tools	5 marks
2.	Transform RTL representation into Logical description	5 marks
3.	Design flow chart for VHDL circuit	5 marks
4.	Design Mealy State machine for a simple counter	5 marks
5.	Why Digital simulation is required to verify the design.	5 marks
	PART B (Answer any five questions)	
6.	Draw Y chart of Electronic Design Automation and explain	7 marks
7.	Design with Logic Symbols of one stage Transistor amplifier using PSPICE	7 marks
8.	Make 4 bit Adder schematic entry in Altera FPGA CPLD EDA system	7 marks
9.	Write Standard Description Languages to Interface a Hex to 7 segment decoder	7 marks
10.	Write Dual Digit Conversion Hex to 7Segment using Standard Description Languages	7 marks
11.	Write VHDL code for D Flip Flop which can be synthesized with 1) synchronous reset 2) an asynchronous Reset	7 marks
12.	Write PSPICE program to simulate operational amplifier	7 marks

Syllabus

Module I - The Concept of Electronic Design Automation - Design Methodology, Development steps, Implementation and Verification, Top Down or Bottom Up, EDA Tools

Module II - Symbolic Design Entry - The Role of Symbolic Design Entry, Schematic Editors, Net-list Generation, Examples of Schematic Entry, Example of an FPGA/CPLD Design, Example of a Printed Circuit Board Design, Example of a Cell Design for Integrated Circuits

Module III - Design using Standard Description Languages – VHDL Design Cycle, Structure of a VHDL Design, Concurrent Statements, The simulation model in VHDL, Process, Sequential clock synchronous logic, Types, Operators, Sub-programs, Test Bench, Packages and Libraries, Advanced VHDL

Module IV - Graphical Specification of System Behavior - Ways of Graphical Descriptions, Partitioning, Optimization, The Concept of Design Re-Use, Design with Virtual Components and Processor Cores, EDA Systems for Hardware/Software Co-Design, System on Chip Designs (SOC),

Module V - Modelling and Verifications - Integrated Circuits and Simulation Model, Structure of a Digital Simulator, Fault Simulation for Verification of Fault Coverage of Test Stimuli, Verification of Testability with Simulation, Necessity of Various Design Tools in the Design Process, Limits of Digital Simulation and Treatment of Complex Circuits.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module -I The Concept of Electronic Design Automation**	
1.1	Design Methodology	**3**
1.2	Development steps	**3**
1.3	Implementation and Verification	**2**
2	**Module II - Symbolic Design Entry**	
2.1	The Role of Symbolic Design Entry	**3**
2.2	Schematic Editors	**3**
2.3	Netlist Generation	**2**
3	**Module III - Design using Standard Description Languages**	
3.1	Structure of a VHDL Design.	**3**
3.2	Concurrent Statements	**3**
3.3	The simulation model in VHDL	**2**
4	**Module IV - Graphical Specification of System Behavior**	
4.1	Ways of Graphical Descriptions	**3**
4.2	Synthesis	**3**
4.3	Hardware/Software Co-Design	**2**
5	**Module V - Modelling and Verifications**	
5.1	Circuit Verification	**3**
5.2	Analog Simulation	**3**
5.3	Digital Simulation	**2**

Text Books

1. The Electronic Design Automation Handbook Dirk Jansen et al Springer Science Publishers
2. Weste, N.; Eshraghian, K.: 'Principles of CMOS VLSI design', Addison-Wesley, 1993

Reference Books

1. J. Rabaey, Digital Integrated Circuits, Prentice Hall, 1996
2. Gajski, D. D.; Kuhn, R. H.: 'Guest Editors Introduction - New VLSI Tools', IEEE Computer
3. Gajski, D. D.: 'Silicon Compilation', Addison-Wesley, 1988

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC064	PYTHON PROGRAMMING FOR EMBEDDED APPLICATIONS	PROGRAM ELECTIVE 1	3	0	0	3

Preamble: Python is the need of the hour – not only for fuelling websites but also for embedded applications. The reason for such spiking popularity is it's easy to download attribute – open source Python programming language can be downloaded for diverse platforms, including Windows and Linux. Moreover, several integrated development environments (IDEs) already exist for Python. Python opens a world of opportunity, including providing support to numerous programming platforms and readable and manageable code. Micro Python aims to be as compatible with normal Python as possible to allow you to transfer code with ease from the desktop to a microcontroller or embedded.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding ofthe fundamentals of Python programming.(Cognitive knowledge level: **Understand**)
CO 2	Attain comprehensive understanding of the modules, package and library concepts of python Programming. (Cognitive knowledge level: **Understand**)
CO 3	Attain comprehensive understanding of the fundamentals of MicroPython programming.(Cognitive knowledge levels: **Understand, analyse, &create**)
CO 4	Attain comprehensive understanding of Micropython on Embedded hardware (Cognitive knowledge levels: **Understand, analyse, create and apply**)
CO 5	Attain comprehensive understanding of Have hands on experience in Micropython based application development (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Attain comprehensive understanding of developing Case studies with Micropython. (Cognitive knowledge levels: **Understand & Apply**)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7

CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	**End Semester Examination**
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge,

derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **222EEC007**	***Course Name:*** **Python Programming for Embedded Applications**	
Time : 2.5 Hours		Maximum : 60 Marks

	PART A (Answer all questions)	
1.	How to create functions in Python. Explain with suitable examples	5 marks
2.	Discuss about the Imaging Libraries for Python.	5 marks
3.	Discuss the Micropython workflow.	5 marks
4.	Briefly discuss the Micropython Supported hardwares for embedded applications.	5 marks
5.	Discuss the MicroPython code style guidelines and idioms	5 marks
	PART B (Answer any five questions)	
6.	Write down the example of how condition statements and looping statements can be used in python	7 marks
7.	How to implement socket based communication using python. Explain with suitable example.	7 marks
8.	Discuss the usage of REPL, Command-Line Tools	7 marks
9.	Discuss the features of Micropython	7 marks
10.	Discuss the procedure for Micro python on Embedded development board?	7 marks
11.	Discuss the procedure and steps to create a Smart alarm system using micro python	7 marks
12.	Discuss the procedure and steps to create a Smart Weather station using micro python	7 marks

Syllabus

Module1: Introduction to Python Programming

Introduction to scripting language, Parts of Python Programming Language, Control Flow Statements, Functions, Strings - Lists - Dictionaries - Tuples and Sets.

Module2: Modules, packages and Libraries in Python

Python Modules and Packages - Creating Modules and Packages, Libraries for Python - Library for Mathematical functionalities and Tools, Networking Libraries, Numerical Plotting Library - GUI Libraries for Python - Imaging Libraries for Python.

Module3: Micropython for Embedded System

Introduction to Micropython, Micropython workflow, REPL, Command-Line Tools, Micropython IDE and programming, Circuit python.

Module4: Micropython on Embedded hardware

Overview of Micropython Supported hardwares, Setting UpMicropython on Embedded development board, Setting Up Micropython on Embedded development board, Creating and deploying Micropython Code, Interfacing sensors, actuators.

Module5: Case studies and Advanced applications

Idiomatic Micropython, Thunder Bot, Racer bot, Sound and Music - Micropython, Smart Weather station, Smart Joke Machine

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module1: Introduction to Python Programming**	
1.1	Introduction to scripting language, Parts of Python Programming Language	**1**
1.2	Control Flow Statements	**1**
1.3	Functions	**3**
1.4	Strings - Lists - Dictionaries - Tuples and Sets.	**2**
2	**Module2: Modules, packages and Libraries in Python**	
2.1	Python Modules and Packages - Creating Modules and Packages	**2**
2.2	Libraries for Python - Library for Mathematical functionalities and Tools.	**3**
2.3	Networking Libraries, Numerical Plotting Library - GUI Libraries for Python - Imaging Libraries for Python	**3**
3	**Module3: Micropython for Embedded System**	
3.1	Introduction to Micropython	**3**
3.2	Micropython workflow	**1**
3.3	REPL, Command-Line Tools	**2**
3.4	Micropython IDE and programming	**2**
3.5	Circuit python	**2**
4	**Module4: Micropython on Embedded hardware**	
4.1	Overview of Micropython Supported hardwares	**1**
4.2	Setting Up Micropython on Embedded development board	**2**
4.3	Creating and deploying Micropython Code	**3**
4.4	Interfacing sensors, actuators	**3**
5	**Module5: Case studies and Advanced applications**	
5.1	Idiomatic Micropython	**2**
5.2	Thunder Bot, Racer bot	**2**
5.3	Sound and Music - Micropython	**2**
5.4	Smart Weather station	**1**
5.5	Smart Joke Machine	**1**

Text Books

1. Gowrishankar S and Veena A, "Introduction to Python Programming", CRC Press, Taylor & Francis Group, 2019
2. Fabrizio Romano, “Learn Python Programming”, Second Edition, Packt Publishing, 2018.

Reference Books

1. Nicholas H. Tollervey, Programming with MicroPython, O'Reilly Media, Inc., 2017
2. Marwan Alsabbagh, MicroPython Cookbook, Packt, 2019

PROGRAM ELECTIVE II

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC108	DATA STRUCTURES AND ALGORITHMS	PROGRAM ELECTIVE 2	3	0	0	3

Preamble: This course includes the basic foundations of data structures and algorithms. It covers the modern theory of algorithms, focusing on the themes of efficient algorithms and intractable problems. Data can be organized in a data structure in such a way that all items may not be required to be searched, and the required data can be searched almost instantly. Algorithm is a step-by-step procedure, which defines a set of instructions to be executed in a certain order to get the desired output. Data Structures are the programmatic way of storing data so that data can be used efficiently. Almost every enterprise application uses various types of data structures.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of basics of data structures (Cognitive knowledge level: **Understand**).
CO 2	Attain comprehensive understanding of how to analyze and establish correctness of algorithms (Cognitive knowledge level: **Understand**).
CO 3	Attain comprehensive understanding of the theory behind various classes of algorithms (Cognitive knowledge levels: **Understand, analyse, &create**)
CO 4	Attain comprehensive understanding of deep data structures and their applications (Cognitive knowledge levels: **Understand, analyse, create and apply**)
CO 5	Attain comprehensive understanding of the theory behind various classes of algorithms (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Attain comprehensive understanding of design, prove the correctness and analyze new algorithms (Cognitive knowledge levels: **Understand & Apply**)

Mapping of course outcomes with program

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-

CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

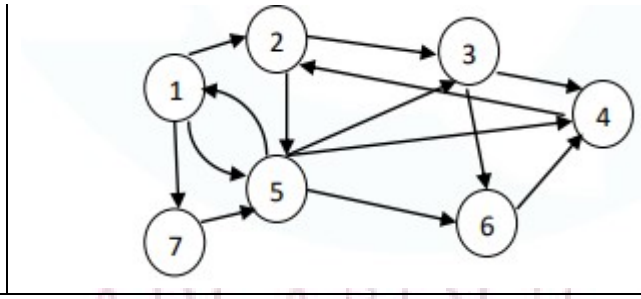
Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

MONTH & YEAR

Course Code: XXXX	***Course Name:*** **Data Structures and Algorithms**
Time : 2.5 Hours	Maximum : 60 Marks

		Marks
	PART A **ANSWER ALL QUESTIONS**	
1	What do you mean by abstract and concrete data structures?	5
2	Write an algorithm to add 2 polynomials of single variable represented using singly linked list.	5
3	Compare Binary Search and Linear Search with the help of algorithms	5
4	Explain any three different hashing functions with an example for each	5
5	Write an algorithm to search for a substring in a given string.	5
	PART B **ANSWER ANY FIVE QUESTIONS**	
6	Define Big-O notation. Derive the Big – O notation for 5n3 +2n2 +3n.	7
7	Compare vectors and arrays in detail	7
8	Assume that a stack is represented using linked list. Write algorithms for the following operations:- (i) Push (ii) Pop	7
9	Write an algorithm/pseudocode to sort elements using Heap sort technique. Illustrate the working of Heap sort algorithm on the following input : 35,15,0,1,60,5,21.	7
10	Write an algorithm to perform binary search on a given set of 'n' numbers. Using the algorithm search for the element 23 in the set [12, 23, 34, 44, 48, 53,87,97]	7
11	Write algorithms for DFS and BFS traversal on a graph	7
12	Write the output of DFS and BFS traversals on the following graph considering starting vertex as 1	7



Syllabus

Module1:Data Structures and Algorithms

Amortized Analysis – aggregate, accounting and potential methods, Data structures: binomial heap, Fibonacci heap, disjoint sets - applications, Number-Theoretic algorithms: GCD algorithm, Extended Euclid's algorithm, Primality testing, Miller-Rabin test, Integer factorization - Pollard Rho heuristic.

Module2: Network flow algorithms

Network flow algorithms: flow properties, augmenting path, Ford-Fulkerson method, Edmonds-Karp heuristics, Maxflow-mincut theorem, push-relabel, relabel-to-front algorithms.

Module3: String matching and Complexity Classes

String matching: Rabin-Karp, Knuth-Morris-Pratt algorithms, Overview of Complexity classes – P, NP, Co-NP, NP-hard, NP-complete, Space complexity.

Module4:Probabilistic algorithms and Complexity classes in randomized algorithms

Probabilistic algorithms: Numerical algorithms: Integration, Counting, Monte-Carlo algorithms - verifying matrix multiplication, min-cut in a network, Las Vegas algorithms, selection sort, quick sort, Dixon's factorization, Complexity classes in randomized algorithms – RP, PP, ZPP, BPP.

Module5: Geometric Algorithms

Geometric Algorithms: Plane sweep technique, role of sweep- line status and event-point schedule, line segment intersection problem, Convex Hull : Graham's scan algorithm, Jarvis March algorithm, Finding closest pair of points, proof of correctness.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module1:Data Structures and Algorithms**	
1.1	Amortized Analysis – aggregate, accounting and potential methods	**1**
1.2	Data structures: binomial heap, Fibonacci heap, disjoint sets - applications	**2**
1.3	Number-Theoretic algorithms: GCD algorithm, Extended Euclid's algorithm	**2**
1.4	Primality testing, Miller-Rabin test	**2**
1.5	Integer factorization - Pollard Rho heuristic	**2**
2	**Module2: Network flow algorithms**	
2.1	Network flow algorithms: flow properties, augmenting path	**2**
2.2	Ford-Fulkerson method, Edmonds-Karp heuristics	**2**
2.3	Maxflow-mincut theorem	**2**
2.4	push-relabel, relabel-to-front algorithms	**3**
3	**Module3: String matching and Complexity Classes**	
3.1	String matching: Rabin-Karp, Knuth-Morris-Pratt algorithms	**2**
3.2	Overview of Complexity classes – P, NP, Co-NP, NP-hard, NP-complete.	**2**
3.3	Space complexity	**1**
4	**Module4:Probabilistic algorithms and Complexity classes in randomized algorithms**	
4.1	Probabilistic algorithms: Numerical algorithms: Integration, Counting	**2**

4.2	Monte-Carlo algorithms - verifying matrix multiplication, min-cut in a network.	**3**
4.3	Las Vegas algorithms, selection sort, quick sort, Dixon's factorization	**3**
4.4	Complexity classes in randomized algorithms – RP, PP, ZPP, BPP	**2**
5	**Module5: Geometric Algorithms**	
5.1	Geometric Algorithms: Plane sweep technique, role of sweep-line status and event-point schedule, line segment intersection problem.	**3**
5.2	Convex Hull : Graham's scan algorithm, Jarvis March algorithm.	**2**
5.3	Finding closest pair of points, proof of correctness.	**2**

Text Books

1. T. H. Cormen, C. E. Leiserson, R. L. Rivest and C. Stein, "Introduction to algorithms", Prentice-hall of India Private Limited, New Delhi, 2010.
2. Gilles Brassard and Paul Bratley, "Fundamentals of algorithms", Prentice-hall of India Private Limited, New Delhi, 2001.

Reference Books

1. Rajeev Motwani, PrabhakarRaghavan, "Randomized Algorithms", Cambridge University Press, 2000.
2. Ellis Horowitz, SartajSahni and Dinesh Mehta, "Fundamentals Of Data Structures In C++ ", Galgotia Publications, 2006.
3. Dexter C. Kozen, "The Design and Analysis of Algorithms", Springer.
4. Jon Kleinberg and Eva Tardos, "Algorithm Design", Pearson Education, 2006.
5. M. H. Alsuwaiyal, "Algorithms Design Techniques and Analysis", World Scientific Publishing Co. Beijing, 1999.
6. S. K. Basu, "Design Methods and Analysis of Algorithms", Prentice Hall India, 2005.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC065	POWER ELECTRONIC & SYSTEM DESIGN	PROGRAM ELECTIVE 2	3	0	0	3

Preamble:

The objective of this course is to make students understand, practice and apply Power Electronics and Magnetic design principles and insights, to make them capable of independently designing complex Power Electronics systems.

The course covers various facets of Power Electronics system design and focuses on designing from the scratch.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn Converters in Equilibrium (Cognitive knowledge level: Understand)
CO 2	Attain comprehensive understanding of Converter Dynamics and Control (Cognitive knowledge level: Understand).
CO 3	Attain understanding in Design of Magnetics (Cognitive knowledge levels: Understand, analyse, &create)
CO 4	Attain understanding in analysing Modern Rectifiers and Power System Harmonics (Cognitive knowledge levels: Understand, analyse, create).
CO 5	Learn, Design Resonant Converters (Cognitive knowledge levels: Understand, analyse, create & Evaluate).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	-	-	-	-
CO 2	-	3	-	-	-
CO 3	2	-	-	-	3
CO 4	-	3	3	3	-
CO 5	-	-	-	-	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30

Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred): **15 marks**

Course based task/Seminar/Data collection and interpretation: **15 marks**

Test paper, 1 number: **10 marks**

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

U	Slot **[SLOT]**
Reg. No:	Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION

Subject: **221EEC065**	**Power Electronic & System Design**
Time : 2Hr 30 minute	Maximum : 60 Marks

	PART A (Answer all questions)	
1	What is converter and explain about boost converter?	5 marks
2.	Derive the transfer function on a buck converter?	5 marks
3.	Calculate the Maximum Primary Inductance of Transformer for Flyback Converter - Input voltage (VIN) 32V to 78V, Output voltage (VOUT) 12V, Output current (IOUT) 1A,	5 marks
4.	How do Current & Voltage Harmonics Affect the System?	5 marks
5	What is a series resonant converter?	5 marks
	PART B (Answer any five questions)	
6.	Design a buck-boost converter to supply a load of 75 W at 50 V from a 40-V source. The output ripple must be no more than 1percent. Specify the duty ratio, switching frequency, inductor size and capacitor size	7 marks
7.	Analyse Buck Boost Converter Transfer Function	7 marks
8.	Discuss the Effect of Negative Feedback on the Network Transfer Function with examples.	7 marks
9.	Design Inductor for Forward Converter Input voltage (VIN) 24V to 12V	7 marks

	Output voltage (VOUT) 5V Output current (IOUT) 1A, Calculate Winding Loss and Current Density	
10.	Design Transformer for Flyback Converter Input voltage (VIN) 32V to 78V, Output voltage (VOUT) 12V, Output current (IOUT) 1A, Calculate Winding Loss and Current Density	7 marks
11.	Derive equation for Total Harmonic Current Distortion (THDi) and discuss its impact on conductor	7 marks
12.	Derive equation for the Design of the Series Resonant Converter for Minimum Component Stress	7 marks

Syllabus

Module-I Converters in Equilibrium - Principle of stead state converter analysis, Steady state equivalent circuit Modelling, losses and Efficiency, Switch Realization, The Discontinuous Conduction Mode, converter circuits.

Module-II Converter Dynamics and Control - AC Equivalent Circuit Modelling, Converter Transfer Functions, Controller Design, Input Filter Design, AC and DC Equivalent Circuit Modelling of the Discontinuous Conduction Mode, Current Programmed Control.

Module-III Magnetics - Inductor Design - Filter Inductor Design Constraints, Multiple Winding Magnetics Design, Transformer Design - Transformer Design basic Constraints, AC Inductor Design.

Module-IV Modern Rectifiers and Power System Harmonics - Power and Harmonics in Non-sinusoidal Systems -Power Factor, Power Phasors in Sinusoidal Systems Harmonic Currents in Three Phase Systems, AC Line Current Harmonic Standards, Line Commutated Rectifiers - Phase Control, Harmonic Trap Filters, Pulse Width Modulated Rectifiers - Control of the Current Waveform, Single Phase Converter System Incorporating Ideal Rectifiers.

Module-V Resonant Converters - Resonant Conversion-Sinusoidal analysis of Resonant Converter, Soft Switching, Load Dependednt Properties of Resonant Converters Soft Switching - Soft Switching mechanisms of Semiconductor Devices, The Zero current switching Quasi-Resonant Switch cell, Resonant Switch Topologies, Soft Switching in PWM Converters.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module -I** Converters in Equilibrium	
1.1	Principle of stead state converter analysis	**3**
1.2	Steady state equivalent circuit Modelling, losses and Efficiency	**3**
1.3	CAD Design	**2**
2	**Module II -** Converter Dynamics and Control -	
2.1	AC Equivalent Circuit Modelling	**3**
2.2	Converter Transfer Functions	**3**
2.3	CAD Design	**2**
3	**Module III - Magnetics**	
3.1	Inductor Design	**3**
3.2	Transformer Design	**3**
3.3	CAD Design	**2**
4	**Module IV - Modern Rectifiers and Power System Harmonics**	
4.1	Power and Harmonics in Non-sinusoidal Systems	**3**
4.2	Line Commutated Rectifiers	**3**
4.3	Pulse Width Modulated Rectifiers	**2**
5	**Module V - Resonant Converters**	
5.1	Resonant Conversion	**3**
5.2	Soft Switching	**3**
5.3	Simulation of Converters	**2**

Text Books

1. Fundamental of Power Electronics Robert W Erickson, Dragan maksimovic, Kluwer Academic Publishers Second Edition, 2000

2. Power Electronic A First Course Ned Mohan, 1995 Second Edition, Wiley Publisher

Reference Books

1. Power Electronics Devices Circuits and Application Muhammad H. Rashid, Prentice Hall Publisher, Third Edition

2. Power Electronics: Devices, Drivers and Applications B. W. Williams, Palgrave Macmillan Publisher (23 January 1987)

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC104	ADVANCED DATA COMMUNICATION AND NETWORKING	PROGRAM ELECTIVE 2	3	0	0	3

Preamble: This course introduces students to the concepts of advanced data communication and networks. Being the backbone for all the IT based developments; Data Communication and Networks has seen tremendous growth in the past decade. There are new techniques and protocols emerging from time-to-time to cater the requirements of this rapidly growing area. The subject will cover history of Internet development, OSI model layers, error detection and correction, switching, multiplexing, CSMA and routing concepts. The treatment would look at current and upcoming network communications technologies for various applications.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of advanced concepts of data communication. (Cognitive knowledge level: **Understand**)
CO 2	Attain comprehensive understanding of the concepts and technologies used in the data communication domain. (Cognitive knowledge level: **Understand**)
CO 3	Attain comprehensive understanding of protocols used in data communication applications. (Cognitive knowledge levels: **Understand, analyse, &create**)
CO 4	Attain comprehensive understanding of latest trends in data communication and networks. (Cognitive knowledge levels: **Understand, analyse, create and apply**)
CO 5	Attain comprehensive understanding of TCP/IP protocol suite. (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**)
CO 6	Attain comprehensive understanding of various types of computer networks. (Cognitive knowledge levels: **Understand & Apply**)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-

CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	**End Semester Examination**
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	**CIE**	**ESE**	**ESE Duration**
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

Course Code: XXXX	***Course Name:*** Advanced Data Communication and Networks
Time : 2.5 Hours	Maximum : 60 Marks

PART A (Answer all questions)		
1	In the ISO-OSI reference model, what are the functions of the transport layer?	5 marks
2.	What are the functions of the Data Link Layer?	5 marks
3.	Why circuit switching cannot be used for 5 packet transmission? Discuss.	5 marks
4.	What is pure ALOHA protocol? Explain how the throughput of a system is computed. Also explain the relationship plot between throughput	5 marks
5	Differentiate between Link-state and Distance vector routing algorithm. How can flooding be minimized?	5 marks
PART B (Answer any five questions)		
6.	Explain your understanding about OSI and TCP/IP models. Out of these, which reference model is being frequently used?	7 marks
7.	Describe Various error detection and correction techniques. The generator polynomial is x3+x+1. A sender wants to send data 1001 . Generate CRC code.	7 marks
8.	Differentiate between Two Layer Switches, Routers and Three Layer Switches	7 marks
9.	What is CSMA/CD? What is the need of back-off in CSMA/CD? Explain back-off algorithm with the help of an example	7 marks
10.	Differentiate Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum	7 marks
11.	(i) Find the class of the following IP 2 address : • 130 .15 .6 . 8 • 245 .33 .5 . 8 (ii) Find the net id and host id of the 3 following IP addresses. • 114 .35 .2 . 7 • 133 .57 .6 . 8 • 207 .34 .54 . 12	7 marks
12.	What are the main issues in routing ? Illustrate good and bad routing using a plot.	7 marks

Syllabus

Module1: Fundamentals of Data Communication and Networks
Data Communications, Networks and Network Types, Internet History, Standards and Administration, Protocol Layering,TCP/IP protocol suite, OSI Model, Digital Data Transmission, DTE-DCE interface, Data Link Layer: Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol, Error Correction: Error correction single bit, Hamming code,

Module2: Error Detection and Correction
Types of Errors, Redundancy, detection versus correction, Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks, Cyclic Codes: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes, Checksum Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol.

Module3: Switching and Multiplexing
Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch, Multiplexing :Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing, Connecting devices:Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks, Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Gigabit Ethernet.

Module4: Media Access Control (MAC)
Media Access Control (MAC) Sub Layer Random Access, ALOHA, Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation, Polling- Token Passing, Channelization, Frequency Division Multiple Access (FDMA), Time – Division Multiple Access (TDMA), Code – Division Multiple Access (CDMA, Spectrum Spreading: Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum.

Module5: Networks Layer
Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance, IPv4 Address, Address Space, Classful Addressing, Classless Addressing, Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF), Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches, Unicast Routing : Introduction, Routing Algorithms-Distance Vector Routing, Link State Routing, Path Vector Routing, Unicast Routing Protocols- Routing Information Protocol(RIP), Open Short Path First Version 4.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in the third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module1: Fundamentals of Data Communication and Networks**	
1.1	Data Communications, Networks and Network Types	**1**
1.2	Internet History, Standards and Administration	**1**
1.3	Protocol Layering,TCP/IP protocol suite, OSI Model	**1**
1.4	Digital Data Transmission, DTE-DCE interface	**2**
1.5	Data Link Layer: Introduction, Data Link Layer, Nodes and Links, Services, Categories of Links, sub layers, Link Layer Addressing, Address Resolution Protocol	**2**
2	**Module2: Error Detection and Correction**	
2.1	Types of Errors, Redundancy, detection versus correction	**1**
2.2	Coding Block Coding: Error Detection, Vertical redundancy cheeks, longitudinal redundancy cheeks	**2**
2.3	Error Correction: Error correction single bit, Hamming code.	**2**
2.4	Cyclic Codes: Cyclic Redundancy Check, Polynomials, Cyclic Code Encoder Using Polynomials, Cyclic Code Analysis, Advantage of Cyclic Codes	**3**
2.5	Checksum Data Link Control: DLC Services, Data Link Layer Protocols, HDLC, Point to Point Protocol	**2**
3	**Module3: Switching and Multiplexing**	
3.1	Switching: Introduction to Switching, Circuit Switched Networks, Packet Switching, Structure of switch	**2**
3.2	Multiplexing :Multiplexing, Frequency Division Multiplexing, Time Division Multiplexing	**2**
3.3	Connecting devices:Passive Hubs, Repeaters, Active Hubs, Bridges, Two Layer Switches, Routers, Three Layer Switches, Gateway, Backbone Networks	**1**
3.4	Wired LANS: Ethernet Protocol, Standard Ethernet, Fast Ethernet, Gigabit Ethernet, 10 Gigabit Ethernet	**1**
4	**Module4: Media Access Control (MAC)**	
4.1	Media Access Control (MAC) Sub Layer Random Access, ALOHA	**1**
4.2	Carrier Sense Multiple Access (CSMA), Carrier Sense Multiple Access with Collision Detection (CSMA/CD), Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA)	**3**
4.3	Controlled Access- Reservation, Polling- Token Passing, Channelization	**1**

4.4	Frequency Division Multiple Access (FDMA), Time – Division Multiple Access (TDMA), Code – Division Multiple Access (CDMA)	**2**
4.5	Spectrum Spreading: Spread Spectrum-Frequency Hopping Spread Spectrum and Direct Sequence Spread Spectrum	**1**
5	**Module5: Networks Layer**	
5.1	Packetizing, Routing and Forwarding, Packet Switching, Network Layer Performance	**2**
5.2	IPv4 Address, Address Space, Classful Addressing, Classless Addressing	**2**
5.3	Dynamic Host Configuration Protocol (DHCP), Network Address Resolution(NATF)	**1**
5.4	Forwarding of IP Packets, Forwarding based on Destination Address, Forwarding based on Label, Routing as Packet Switches	**2**
5.5	Unicast Routing : Introduction, Routing Algorithms- Distance Vector Routing, Link State Routing, Path Vector Routing, Unicast Routing Protocols- Routing Information Protocol(RIP), Open Short Path First Version 4	**2**

Text Book

1. B. A. Forouzan, “Data Communications and Networking”, 5th, 2013, TMH.

Reference Books

1. William Stallings, “Data and Computer Communications”, 8th ed., 2007, PHI.
2. Prakash C. Gupta, “Data Communications and Computer Networks”, 2006, PHI.
3. B. A. Forouzan, “Data Communications and Networking”, 2nd, 2013, TMH.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC009	SENSOR TECHNOLOGIES AND MEMS	PROGRAM ELECTIVE 2	3	0	0	3

Preamble:

This course aims to impart knowledge on the fundamental aspects of Sensor design and development. It also imparts the development stage using MEMS Technology. When the Integration occurs the design flaws, developmental failures and analysis mismatch occurs. The course covers extensively in all these aspects.

Course Outcomes:

After the completion of the course the student will be able to

CO 1	Study the fundamentals of the sensor. **(Cognitive Knowledge Level: Analyze)**
CO 2	Apply varied parameters in the design of industrial classified sensor **(Cognitive Knowledge Level: Apply)**
CO 3	Evaluate the standards and calibrations of sensors with test and measurements**(Cognitive Knowledge Level: Evaluate)**
CO 4	Study the MEMS in sensor technology **(Cognitive Knowledge Level: Analyze)**
CO 5	Create the unique application-based testing and standards for qualification by performing the failure analysis. **(Cognitive Knowledge Level: Create)**

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	2	-	1	-	-	2	-
CO 2	3	-	1	-	-	2	-

CO 3	3	3	2	3	2	2	1
CO 4	3	-	1	-	-	2	-
CO 5	1	3	3	3	3	2	1

Programme Outcomes

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

TotalMarks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks.

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY FIRST SEMESTER M.TECH DEGREE EXAMINATION			Name Register No:
Course code	221EEC009	Course name	*SENSOR TECHNOLOGIES AND MEMS*
Max. Marks	60	Duration	2.5 Hour

	PART A (Answer ALL questions)	
1	Classify the performance of signal conditioning	5
2	By applying the different parameters give design specifications of capacitive based accelerometer	5
3	Sketch the frequency response of microphone and identify the different parameters.	5
4	Give the microfabrication process and simulation steps in MEMS Design	5
5	What criteria would you use to assess the performance of photovoltaic cells in MEMS based energy measurement.	5
	PART B (Answer any five questions.)	
6	Analyze the sensor characteristics and system characteristics obtained in test lab and Industry Environment.	7
7	How does comparison of the different accelerometers is done?	7
8	Relate the limitations in measurement range.	7
9	Does Quality factor and loss coefficient become a factor in MEMS vibrating structures. Justify.	7
10	Design a electrohydrodynamic applications and analyses the performance parameters for it.	7

11	What is the most important performance index of fuel cells in MEMS based energy measurement.	7
12	How would you decide about the Thermal Shock, Test Method 503.5 . Give a case study.	7

Syllabus

Module 1 – Sensor Fundamentals

Basic Sensor Technologies, Sensor System.Sensor Characteristics, System Characteristics, Instrument Selection,Data Acquisition, Measurement Issues, Sensor Signal Conditioning: Conditioning Bridge Circuits, Amplifiers for signal conditioning,Usage of ADC.Signal Conditioning High Impedance Sensors.Basic Types of Sensors- Acceleration,Shock, Vibration Sensors,Biosensors, Chemical Sensors.

Module 2- Industrial Classified Sensors

Capacitive, Inductive Displacement Sensors,Flow and Level Sensors, Force Load and Weight Sensors,Humidity Sensors, Machinery Vibration Monitoring sensors,Optical and Radiation Sensors,Position and Motion sensors,Pressure Sensors,Sensors for mechanical shock,Temperature sensors, nanotechnology enabled sensors

Module 3- Test and Measurements

Example of Microphone, Characteristics, types of microphones,Formation of frequency response.limitations of measurements range, effects of environmental conditions,Standards and calibrations. Manufactures of test equipment and usage. Strain gauge-based measurements and standards,Applications of wireless sensor networks in measurement and cyber physical systems. Materials used in sensor technology-types, composition, properties and performances.

Module 4- MEMS in Sensor Technology

Microelectromechanical systems design and modelling. Materials, microfabrication process, simulation,Micro actuators: design and technology, micro reaction chambers, resonant frequency response of smart microelectromechanical systems vibrating structures.Quality factor and the loss coefficient of smart microelectromechanical systems vibrating structures.MEMS accelerometers,MEMS gyroscope,MEMS magnetometer, electro hydrodynamic printing applications.

Module 5- MEMS Sensor Applications and Reliability

Photovoltaic and fuel cells in power microelectromechanical systems for smart energy management,MEMS for smart communication systems and future 5G applications,Smart acoustic sensor array system for real time sound processing applications,Failure modes and mechanisms: Failure modes and mechanisms in MEMS,In Use Failures,Root Cause and Failure Analysis,Testing and Standards for Qualification, Continuous improvement: tools and techniques for reliability improvement.

Course Plan

No	Topic	No. of Lectures
1	**Module 1 – Sensor Fundamentals**	
1.1	Basic Sensor Technologies, Sensor System.	1
1.2	Sensor Characteristics, System Characteristics, Instrument Selection,	1
1.3	Data Acquisition, Measurement Issues, Sensor Signal Conditioning: Conditioning Bridge Circuits, Amplifiers for signal conditioning,	1
1.4	Usage of ADC.	1
1.5	Signal Conditioning High Impedance Sensors	1
1.6	Basic Types of Sensors- Acceleration,	1
1.7	Shock, Vibration Sensors	1
1.8	Biosensors, Chemical Sensors	1
2	**Module 2- Industrial Classified Sensors**	
2.1	Capacitive, Inductive Displacement Sensors	1
2.2	Flow and Level Sensors, Force Load and Weight Sensors	1
2.3	Humidity Sensors, Machinery Vibration Monitoring sensors,	1
2.4	Optical and Radiation Sensors,	1
2.5	Position and Motion sensors	1
2.6	Pressure Sensors	1
2.7	Sensors for mechanical shock	1
2.8	Temperature sensors, nanotechnology enabled sensors	1
3	**Module 3- Test and Measurements**	
3.1	Example of Microphone, Characteristics, types of microphones,	1

3.2	Formation of frequency response	1
3.3	limitations of measurements range, effects of environmental conditions,	1
3.4	Standards and calibrations	1
3.5	Manufactures of test equipments and usage	1
3.6	Strain gauge-based measurements and standards,	1
3.7	Applications of wireless sensor networks in measurement and cyber physical systems	1
3.8	Materials used in sensor technology-types, composition, properties and performances	1
4	**Module 4- MEMS in Sensor Technology**	
4.1	Microelectromechanical systems design and modelling	1
4.2	Materials, microfabrication process, simulation,	1
4.3	Micro actuators: design and technology, micro reaction chambers, resonant frequency response of smart microelectromechanical systems vibrating structures	1
4.4	Quality factor and the loss coefficient of smart microelectromechanical systems vibrating structures.	1
4.5	MEMS accelerometers	1
4.6	MEMS gyroscope	1
4.7	MEMS magnetometer	1
4.8	electrohydrodynamic printing applications	1
5	**Module 5- MEMS Sensor Applications and Reliability**	
5.1	Photovoltaic and fuel cells in power microelectromechanical systems for smart energy management	1
5.2	MEMS for smart communication systems and future 5G applications,	1
5.3	Smart acoustic sensor array system for real time sound processing applications	1
5.4	Failure modes and mechanisms: Failure modes and	1

	mechanisms in MEMS	
5.5	In Use Failures	1
5.6	Root Cause and Failure Analysis	1
5.7	Testing and Standards for Qualification	1
5.8	Continuous improvement: tools and techniques for reliability improvement	1

Text Books

1. Jon S Wilson, *Sensor Technology Handbook*, Newnes,2005
2. S Nihtianov, A. Luque,*Smart Sensors and MEMS*,*Woodhead Publishing*,2013

ReferenceBooks

1. Horst czihos, Measurement, *Testing and Sensor Technology*, Springer, 2011
2. Allyson L Hartzell, Mark G dasilva, Herbert R.Shea, *MEMS Reliability*,Springer, 2011
3. Tina L. Lamers, Beth L. Pruitt (auth.), Reza Ghodssi, Pinyen Lin (eds.), *MEMS Materials and Processes Handbook*,Springer , 2011
4. Brand Fedder, *System level modelling of MEMS*, Wiley-VCH, 2013
5. Sergey Y. Yurish, Maria Teresa S. R. Gomes , *Smart Sensors and MEMS*, Springer, 2004

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC066	FLEXIBLE ELECTRONICS	PROGRAM ELECTIVE 2	3	0	0	3

Preamble:

Flexible and large-area electronics has the potential to mark a further technology revolution in electronics – much like the way the transition from circuits based on discrete components to integrated circuits did – by enabling the pervasive integration of electronic functionalities in all sorts of appliances, their portability, and wearability.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Flexible Electronics Technology
CO 2	Thin Film Transistors
CO 3	Flexible Transition Metal Oxide Electronics
CO 4	Amorphous Silicon
CO 5	Sheet type Sensors and Actuators
CO 6	Flexible Photo Voltaic Fabrication

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	1	-	-	-	-	-
CO 2	-	2	-	-	-	-
CO 3	-	-	3	2	1	3
CO 4	3	-	-	3	-	-
CO 5	-	1	2	-	3	-
CO 6	-	-	-	-	-	1

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10

Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred): 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 number: 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

U	Slot **[SLOT]**
Reg. No:	Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
FIRST SEMESTER M.TECH DEGREE EXAMINATION

Subject: *09ECXXXX*	***FLEXIBLE ELECTRONIC***
Time : 2Hr 30 minute	Maximum : 60 Marks

	PART A (Answer all questions)	
1	Briefly discuss the type of Materials used in Flexible Electronics	5 marks
2.	List the advantages of Nano-crystalline Silicon Materials	5 marks
3.	Write short notes on Flexible Backplanes and Displays	5 marks
4.	Discuss Sheet Type Braille Displays	5 marks
5	What is an organic Photovoltaics? Discuss in detail.	5 marks
	PART B (Answer any five questions)	
6.	With proper depiction illustrate the Mechanical Theory of Film on Substrate Foil Structure	7 marks
7.	Explain Novel Patterning Methods for Flexible Electronics	7 marks
8.	Describe Low Temperature Dielectrics	7 marks
9.	Describe Flexible Transition Metal Oxide Electronics	7 marks
10.	Describe Flexible Active Matrix Backplanes	7 marks
11.	Describe Flexible sensors for biomedical applications	7 marks
12.	Describe Flexible Glass in Thin Film Photovoltaics	7 marks

Syllabus

Module 1: Flexible Electronics Technology

Materials for Flexible Electronics, Fabrication Technology for Flexible Electronics, Mechanical Theory of Film on Substrate Foil Structure, Materials and Novel Patterning Methods for Flexible Electronics.

Module2: Thin Film Transistors

Low Temperature Amorphous and Nano-crystalline Silicon Materials, Low Temperature Dielectrics, Low Temperature Thin Film Transistor Devices, Flexible Transition Metal Oxide Electronics.

Module3: Amorphous Silicon

Flexible Backplanes and Displays, Flexible Active Matrix Backplanes, Flexible AMOLED Displays.

Module 4: Sheet type Sensors and Actuators

Sheet type Image Scanners, Sheet Type Braille Displays, Flexible sensors for biomedical applications.

Module 5: Flexible Photo Voltaic Fabrication

Physics and Materials issues of organic Photovoltaics, PV fabrication on Flexible Substrates, Flexible Glass in Thin Film Photovoltaics.

Corse Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	Flexible Electronics Technology	
1.1	Materials for Flexible Electronics	2
1.2	Fabrication Technology for Flexible Electronics	2
1.3	Mechanical Theory of Film on Substrate Foil Structure	2
1.4	Materials and Novel Patterning Methods for Flexible Electronics	2
2	Thin Film Transistors	
2.1	Low Temperature Amorphous and Nano-crystalline Silicon Materials	
2.2	Low Temperature Dielectrics	3
2.3	Low Temperature Thin Film Transistor Devices	3
2.4	Flexible Transition Metal Oxide Electronics	2
3	Amorphous Silicon	
3.1	Flexible Backplanes and Displays	3
3.2	Flexible Active Matrix Backplanes	3
3.3	Flexible AMOLED Displays	2
4	Sheet type Sensors and Actuators	
4.1	Sheet type Image Scanners	3
4.2	Sheet Type Braille Displays	3
4.3	Flexible sensors for biomedical applications	2
5	Flexible Photo Voltaic Fabrication	
5.1	Physics and Materials issues of organic Photovoltaics	2
5.2	PV fabrication on Flexible Substrates	3
5.3	Flexible Glass in Thin Film Photovoltaics	3

Text Book

1. Electronic Materials Science and Technology Harry L Tuller, Springer

Reference Books

1. Flexible Electronics Fabrication and Ubiquitous Integration, Ramses V. Martinez, **Mdpi AG**

2. Environmental Chemical and Medical Sensors Shantanu Bhattacharya, Avinash Kumar Agarwal, Nripen Chanda, Ashok Pandey, Ashis Kumar Sen

3. Flexible Glass Enabling Thin, Lightweight and Flexible Electronics, Sean M Garner, Wiley

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
221EEC067	VLSI SYSTEM DESIGN	PROGRAM ELECTIVE 2	3	0	0	3

Preamble:

The objective of this course is to make students understand, practice and apply VLSI System design principles and insights, to make them capable of independently designing complex digital systems..

The course covers various facets of CMOS VLSI digital system design and focuses on designing from the scratch. The course focuses on designing CMOS combinational and sequential building blocks, using these building blocks to design complex digital systems

Course Outcomes:

After the completion of the course the student will be able to

CO 1	Attain comprehensive MOS Transistor Theory and device Characteristics. (Cognitive knowledge level: **Understand**).
CO 2	Attain comprehensive understanding of CMOS digital logic design fundamentals (Cognitive knowledge level: **Understand**).
CO 3	Attain understanding in designing and analysing combinational circuit and subsystems (Cognitive knowledge levels: **Understand, analyse, create**).
CO 4	Attain understanding in designing and analysing sequential circuit and subsystems (Cognitive knowledge levels: **Understand, analyse, create).**
CO 5	Enable design of arithmetic circuits, data path units and control units for microcomputer designs (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Understand VLSI digital logic testing methods for reliability and their applications. Cognitive knowledge levels: **Understand & Apply**).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1							
CO 2			2		3		
CO 3			2		3	2	
CO 4			2		3	2	
CO 5			2			3	
CO 6			2			2	

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

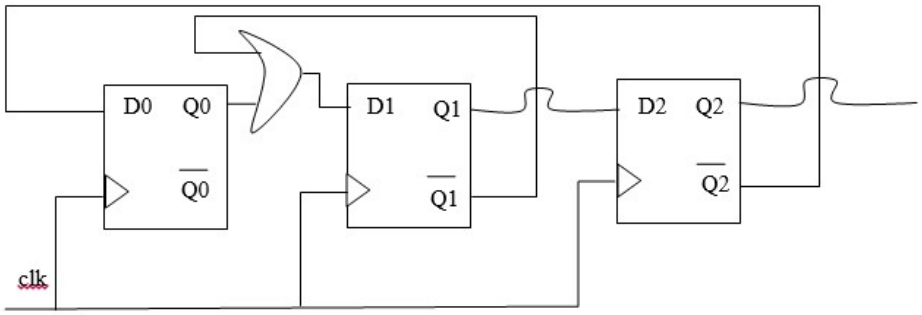
Continuous Assessment - Test: 30 marks
Continuous Assessment - Assignment: 10 marks

End Semester Examination Pattern:

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

PART A (Answer all questions)		
1	Explain the basic structure, operation and drain current characteristics of a depletion type MOSFET.	5 marks
2.	Explain the design procedure for combinational circuits with an example	5 marks
3.	Explain the term 'Meta-stability' and how it can be avoided?	5 marks
4.	Convert the following numbers i)(163.789)10 to Octal number ii)(11001101.0101)2 to base-8 and base-4 iii)(4567)10 to base2 iv) (4D.56)16 to Binary	5 marks
5	Discuss the design for testability and different fault models	5 marks
PART B (Answer any Five questions)		
6.	Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.	7 marks
7.	Classify different types of MOS scaling. Derive their effects on various parameters of MOSFET.	7 marks
8.	Explain the operations of a basic 4 bit adder, describe the different approaches of improving the speed of adder.	7 marks
9.	Given the following circuit. Assume initially all flip-flops are cleared. After the 5th clock edge the value of Q2,Q1,Q0 is _____. Draw timing and verify the same. Given $t_{\_setup}$= 4n ses, $t_{\_pd}$= 6nsec, $t_{\_hold}$ = 4n sec, $t_{\_gate}$= 5n sec. t_skewD1flop=4nsec, t_seskewD2flop = 7nsec. Find the maximum frequency of operation without any timing violations.	7 marks

		
10.	Design a circuit which transfers a single clock wide pulse from 100 Mhz clock domain and create a single clock wide pulse in 5 MHz clock domain. Assume 100 MHz and 5 MHz clocks are asynchronous.	7 marks
11.	Design a sequence detector circuit to detect 1010 with overlapping seq.	7 marks
12.	With proper depiction explain Built-in Self-test.	7 marks

Syllabus

Module 1: CMOS LOGIC DESIGN FUNDAMENTALS

MOS Transistor Theory, MOS Regions of Operations, Device Equations, Device Scaling, Charateristics.

Module 2: COMBINATIONAL LOGIC DESIGN

Functional blocks – Multiplexers,Decoders, Encoders, Tri-state devices, , Parity circuits, Comparators, Adders, sub tractors, carry look- ahead adder, timing analysis. Combinational multiplier structures. Timing hazards.

Module 3: SEQUENTIAL LOGIC DESIGN

Latches and Flip-Flops, Sequential logic circuits – timinganalysis (Set up and hold times) Synchronizers and met stability. State machines – Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning; FSM Design examples.

Module 4: DIGITAL SUBSYSTEMS

ALU, 4-bit combinational multiplier, Barrel shifter, Pattern (sequence) detector, Programmable Up-down counter, Round robin arbiter with 3 requesters
Process Controller, FIFO.

Module 5: DIGITAL VLSI Logic TESTING

Introduction to digital VLSI testing, Fault modelling, fault collapsing, fault simulation, test generation, Introduction to Design For Testability(DFT),DFT and Built-In-Self-Test(BIST).

Corse Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**CMOS LOGIC DESIGN FUNDAMENTALS**	
1.1	MOS Transistor Theory	**1**
1.2	MOS Regions of Operations, Device Equations	**3**
1.3	Device Scaling, Charateristics	**3**
2	**COMBINATIONAL LOGIC DESIGN**	
2.1	Functional blocks – Multiplexers,Decoders, Encoders, Tri-state devices, , Parity circuits, Comparators,	**3**
2.2	Adders, sub tractors, carry look- ahead adder, timing analysis. Combinational multiplier structures.	**4**
2.3	Timing hazards	**1**
3	**SEQUENTIAL LOGIC DESIGN**	
3.1	Latches and Flip-Flops, Sequential logic circuits – timinganalysis (Set up and hold times) Synchronizers and met stability.	**2**
3.2	State machines – Mealy & Moore machines, Analysis, FSM design using D Flip-Flops, FSM optimization and partitioning;	**4**
3.3	FSM Design examples	**2**
4	**DIGITAL SUBSYSTEMS**	
4.1	Arithmetic Operations Floating Point Number system – IEEE 754 format & POSIT Basic binary codes. Simple fixed point to floating point encoder	**2**
4.2	ALU, 4-bit combinational multiplier, Barrel shifter,	**2**
4.3	Pattern (sequence) detector, Programmable Up-down counter, Round robin arbiter with 3 requesters Process Controller, FIFO	**4**
5	**DIGITAL VLSI Logic TESTING**	
5.1	Introduction to digital VLSI testing	**2**
5.2	Fault modelling, fault collapsing, fault simulation, test generation	**4**
5.3	Introduction to Design For Testability(DFT),DFT and Built-In-Self-Test(BIST)	**2**

Text Books

1. Jan M.Rabaey ,“Digital Integrated Circuits” , 2nd edition, September, PHl
2. Douglas A.Pucknell,”Basic VLSI design”, PHI Limited.

Reference Books

1. CMOS VLSI Design: A Circuits and Systems Perspective Hardcover by Neil Weste, David Harris, Person Education .
2. CMOS Logic Circuit Design, by John P. Uyemura, Springer.
3. Circuit Design for CMOS VLSI by John P. Uyemura, Springer.
4. CMOS Digital Integrated Circuits, Analysis and Design by Sung-Mo Kang, Yusuf Leblebici, Chulwoo Kim,McGraw Hill.
5. E.Fabricious, "Introduction to VLSI design", Mc Graw Hill
6. Digital Design by M. Morris R. Mano and Michael D. Ciletti.,Person Education.
7. Digital Design by Frank, John Wiley and Sons Publishers.
8. Digital Computer Arithmetic Datapath Design Using Verilog HDL by James E. Stine, Spinger
9. Gustafson and Yonemoto. 2017. Beating Floating Point at its Own Game: Posit Arithmetic. Supercomputing Frontiers and Innovations: an International Journal, Volume 4I, ssue 2, June 2017 , pp 71–86, https://doi.org/10.14529/jsfi170206.
10. Digital Design Principles and Practices by John F. Wakerly, Pearson Education.
11. An Introduction to Logic Circuit Testing by Parag K. Lala, Morgan & Claypool Publishers.
12. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits by M. Bushnell , Vishwani Agrawal,Springer.
13. Digital Systems Testing and Testable Design by Melvin A. Breuer , Arthur D. Friedman, Miron Abramovici, Wiley-IEEE Press

CODE 221LEC006	COURSE NAME SYSTEM DESIGN USING EMBEDDED PROCESSORS LAB	CATEGORY	L	T	P	CREDIT
		Laboratory	0	0	2	1

Preamble: Embedded systems are normally built around Microcontrollers and ARM Processor based SOCs. This Embedded System using Embedded Processor course focuses on the architecture and programming of embedded processors. The objective of the course is to provide understanding of the techniques essential to the design and implementation of embedded systems using suitable hardware and software tools. This course offers a range of topics of immediate relevance to industry and makes the participants exactly suitable for Embedded Industry.

Course Outcomes:

After the completion of the course the student will be able to

CO 1	ARM assembly language Programming.
CO 2	Perform ARM Cortex M4 Microcontroller configuration for various applications using peripheral devices.
CO 3	Perform ARM Cortex M4 Microcontroller using interrupt and DMA based peripheral configuration.
CO 4	Demonstrate an embedded system on ARM Cortex M4 Microcontroller development boards.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	2	-	-
CO 2	1	1	-	3	2	-	-
CO 3	2	-	2	3	-	-	-
CO 4	1	-	2	3	-	-	-

Assessment Pattern

Bloom's Category	Continuous Evaluation
Apply	40
Analyse	20
Evaluate	20
Create	20

Mark distribution

Total Marks	CIE	ESE
100	100	-

Continuous Internal Evaluation Pattern: 100 Marks

The laboratory courses will be having only Continuous Internal Evaluation and carries 100 marks. Final assessment shall be done by two examiners; one examiner will be a senior faculty from the same department.

List of Experiments

Sl. No	CO Mapping	Practical Exercises (60 Hours)
1	CO1	ARM Assembly Language Programming
2	CO2	Embedded C Programming on ARM Cortex M4 Microcontroller with CMSIS/HAL libraries
3	CO2, CO3	Embedded C Programming - Peripheral Programming - GPIO, ADC, DAC
4	CO2, CO3	Embedded C Programming - ARM Cortex M4 Peripheral Programming - USART, UART
5	CO3,CO4	Embedded C Programming - Peripheral Programming - I2C, SPI
6	CO2, CO3	Embedded C Programming - ARM Cortex M4 Peripheral Programming - Timers, Watchdog Timers
7	CO2, CO3	Embedded C Programming - ARM Cortex M4 Peripheral Programming - PWM
8	CO3	Embedded C Programming - ARM Cortex M4 Peripheral Programming - Interrupt Handling
	CO2, CO3	Embedded C Programming - ARM Cortex M4 Peripheral Programming - USB, CAN
	CO2, CO3	Embedded C Programming - ARM Cortex M4 Peripheral Programming - DMA

9	**CO2, CO3,CO4**	Design of a real-time data acquisition & control system using the ARM Cortex M4 Microcontroller

Reference Books

1. Yiu J. The Definitive Guide to ARM Cortex M3 and Cortex M4 Processors, 3rd Edition, Elsevier
2. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier
3. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education
4. Cortex-M4 Technical Reference Manual (TRM)
5. Raj Kamal, “Microcontroller - Architecture Programming Interfacing and System Design” 1st Edition, Pearson Education
6. P.S Manoharan, P.S. Kannan, “Microcontroller based System Design”, 1st Edition, Scitech Publications
7. STMicroelectronics Nucleo-G4xx development board user manual

SEMESTER II

Discipline : Electronics and Communication Engineering
Stream : EC8

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222TEC100	FOUNDATIONS OF DATA SCIENCE	DISCIPLINE CORE 2	3	0	0	3

Preamble: Nil

Course Outcomes: After the completion of the course the student will be able to

CO 1	Understand the basics of machine learning and different types.
CO 2	Differentiate regression and classification, Understand the basics of unsupervised learning and non-metric methods
CO 3	Apply statistical methods in non-linear classification and neural networks
CO 4	Understand the basics of deep learning networks, convolutional neural networks

Mapping of course outcomes with program outcomes (1-3)

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	2	1	2	3	3	2	2
CO 2	2	2	2	2	2	2	2
CO 3	2	1	2	3	3	1	1
CO 4	2	1	2	3	3	1	1

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation : 40 marks
Micro project/Course based project : 20 marks
Course based task/Seminar/Quiz : 10 marks
Test paper, 1 no. : 10 marks

End Semester Examination Pattern:
Total : 60 marks
Part A: Answer all – 5 questions x 5 marks : 25 marks
Part B: Answer 5 of 7: 5 questions x 7 marks : 35 marks

The end semester examination will be conducted by the University . There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

Total: 60 marks

Part A (Answer all) 25 marks

1. Discuss different types of machine learning with examples. (5)
2. Differentiate regression and classification with examples (5)
3. How SVM is used for multiclass problem? (5)
4. Explain clustering with examples. (5)
5. Discuss different activation functions used in deep neural networks (5)

Part B (Answer any 5) 35 marks

6. Explain the terms features, training set, target vector, test set, and curse of dimensionality in machine learning. (7)
7. Show that the Bayesian classifier is optimal with respect to minimizing the classification error probability. (7)
8. Give a step by step description of the perceptron algorithm in classification. (7)
9. Obtain the cost function for optimization in SVM for separable classes. (7)
10. Describe convolutional neural networks with detailed description of each layers (7)
11. Obtain the decision surface for an equi-probable two class system, where the probability density functions of n-dimensional feature vectors in both classes are normally distributed. (7)
12. Explain the principle of back propagation neural networks with neat architecture diagram (7)

Syllabus and Course Plan (total hours: 37)

No	Topic	hours
1	**8 hours**	
1.1	Basics of machine learning, supervised and unsupervised learning,examples,	2
1.2	features, feature vector, training set, target vector, test set	1
1.3	over-fitting, curse of dimensionality.	1
1.4	Evaluation and model selection: ROC curves, evaluation measures,	2
1.5	validation set, bias-variance trade-off.	1
1.6	confusion matrix, recall, precision, accuracy.	1
2	**7 hours**	
2.1	Regression: linear regression, error functions in regression	1
2.2	multivariate regression, regression applications, bias and variance.	1
2.3	Classification : Bayes' decision theory,	2
2.4	discriminant functions and decision surfaces,	1
2.5	Bayesian classification for normal distributions, classification applications.	2
3	**7 hours**	
3.1	Linear discriminant based algorithm: perceptron, perceptron algorithm,	1
3.2	support vector machines.	2
3.3	Nonlinear classifiers, the XOR problem,	2
3.4	multilayer perceptrons,	1
3.5	backpropagation algorithm.	1
4	**8 hours**	
4.1	Unsupervised learning:	1
4.2	Clustering, examples, criterion functions for clustering,	2
4.3	proximity measures, algorithms for clustering.	1
4.4	Ensemble methods: boosting, bagging.	2
4.5	Basics of decision trees, random forest, examples.	2
5	**7 hours**	
5.1	Introduction to deep learning networks,	1
5.2	deep feedforward networks,	2
5.3	basics of convolutional neural networks (CNN)	2
5.4	CNN basic structure, Hyper-parameter tuning, Regularization - Dropouts,	1
5.5	Initialization, CNN examples	1

Reference Books

1. Bishop, C. M. "Pattern Recognition and Machine Learning" Springer, New York, 2006.
2. Theodoridis, S. and Koutroumbas, K. "Pattern Recognition". Academic Press, San Diego, 2003.
3. Hastie, T., Tibshirani, R. and Friedman, J. "The Elements of Statistical Learning". Springer.

4. Duda, R.O., Hart, P.E., and Stork, D.G. “Pattern Classification”. Wiley, New York,

5. Ian Goodfellow, Yoshua Bengio, Aaron Courville. “Deep Learning” MIT Press, 2016

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222TEC007	RECONFIGURABLE COMPUTING	PROGRAM CORE 3	3	0	0	3

Preamble: Recent advances in data analytics, machine learning, artificial intelligence, etc. technologies have made a leap in computational requirement. Hence, for implementing practical applications of those technologies, hardware acceleration is essential. Further, the advances in VLSI technology have given upswing to a fresh class of computer architectures which take advantage of application-level parallelism. These reconfigurable computers can be quickly customized at the hardware level to perform exactly the computation required in hardware, overcoming the fixed hardware configurations found in many contemporary microprocessors. This course, covers the state-of heart in reconfigurable computing both from a hardware and software perspective.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Able to select suitable hardware for an application
CO 2	Able to understand the design methodology of micro-processor system on Chip (SoC) buses, memory peripherals on FPGA
CO 3	Build reconfigurable system using FPGAs
CO 4	Able to evaluate hardware accelerator and achieve acceleration factor for a specific application.
CO 5	Perform partial reconfiguration for various applications using peripheral devices.
CO 6	Demonstrate an embedded system on FPGA using IP blocks.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	-	1	-	-	3	-	-
CO 2	-	2	-	-	2	-	-
CO 3	2	-	2	3	-	-	-
CO 4	2	-	2	-	-	-	-
CO 5	1	-	-	2	3	2	-
CO 6	2	-	2	3	2	2	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	10
Evaluate	10
Create	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: XXXX	***Course Name:*** **Reconfigurable Computing**

Time : 2.5 Hours		Maximum : 60 Marks

	PART A (Answer all questions)	
1	The Xilinx Virtex-7 FPGA comprises an architecture composed of two types of configuration logic blocks (CLBs), namely SLICEM and SLICEL blocks. Explain what a CLB is – surely it is just the same as a LUT (or is it)? Discuss the differences between SLICEL and SLICEM blocks and how different slides can be beneficial in terms of FPGA manufacture and programming.	5 marks
2.	Briefly describe the methodology of System on Chip devices on FPGA.	5 marks
3.	With proper timing illustrate AXI Lite bus protocol.	5 marks
4.	With proper depiction describe co-processor interfacing techniques.	5 marks
5	List the advantages of high level synthesis.	5 marks

	PART B (Answer any Five questions)	
6.	With proper depiction, briefly describe the classification of reconfigurable architectures.	7 marks
7	Briefly describe various SoC design platforms and detail the system implementation challenges.	7 marks
8.	With proper depiction, detail Xilinx Zynq 7000 programmable SoC architecture.	7 marks
9.	With proper depiction and timing detail interfacing an AXI peripheral to a processor core.	7 marks
10.	Briefly describe various debugging methodologies on an FPGA based SoC development platform.	7 marks
11.	Detail various steps in emulating a multi-core SoC on FPGA.	7 marks
12.	Detail various steps involved in creating and interfacing an FFT accelerator core to ARM A9 processor on the Zynq SoC platform.	7 marks

Syllabus

Module-I: Introduction to Reconfigurable Computing

Reconfigurable Architectures: Classification of Reconfigurable Architectures.FPGA Technology and Architectures, LUT devices and Mapping, Placement and Partitioning. Programming Technology: HDL Based Programming and High level Synthesis using C, Partial Reconfiguration.Intellectual Property Based Design: Soft core, Firm core and Hard Core, Software tools.

Module-II: System on chip (SoC) system in FPGA devices

Embedded computer organization and methodology of System on chip (SoC) system in FPGA devices. Design challenges and Differences GPP, DSP, ASIC and FPGA based System On Chip platforms. Application profiling and partitioning, FPGAs vs. Multi-core processor architectures. Xilinx Zynq 7000 family programmable SoC (system on chip) in particular - hybrid device with ARM + FPGA architecture.

Module-III: Overview of AXI Bus protocol

Design of Master and Slave Bus protocols based IPs.Design Metrics, General purpose peripherals (interrupt, timer, clock, DMA etc.) and special purpose peripherals Serial Transmission protocols & Standards, and advanced high speed buses. Debugging methodologies.

Module-IV: Emulating SoC Architectures on FPGAs

Emphasis on different embedded processors and multiprocessor and architectures. Coprocessor creation, hardware design for System-On-a-Chip. Memory and peripheral interfacing. System level design Tradeoffs, Power, Energy, Performance and Area.

Module-V: High level synthesis and system modeling

Overview of high level synthesis (HLS). Exploration of HLS tools, System Modeling. Models of Computation and System Specification Languages, High Level Computation/Behavioral Synthesis. Application case study like FFT, JPEG.

Course Plan

(For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Introduction to Reconfigurable Computing**	
1.1	Reconfigurable Architectures: Classification of Reconfigurable Architectures.	2

1.2	FPGA Technology and Architectures, LUT devices and Mapping, Placement and Partitioning.	2
1.3	Programming Technology: HDL Based Programming and High level Synthesis using C, Partial Reconfiguration.	2
1.4	Intellectual Property Based Design: Soft core, Firm core and Hard Core, Software tools.	2
2	**System on chip (SoC) system in FPGA devices**	
2.1	Embedded computer organization and methodology of System on chip (SoC) system in FPGA devices.	2
2.2	Design challenges and Differences GPP, DSP, ASIC and FPGA based System On Chip platforms.	2
2.3	Application profiling and partitioning, FPGAs vs. Multi-core processor architectures	2
2.4	Xilinx Zynq 7000 family programmable SoC (system on chip) in particular - hybrid device with ARM + FPGA architecture.	2
3	**Bus-protocols and Intellectual Property study**	
3.1	Overview of AXI Bus protocol	2
3.2	Design of Master and Slave Bus protocols based IPs	2
3.3	Design Metrics, General purpose peripherals (interrupt, timer, clock, DMA etc.) and special purpose peripherals Serial Transmission protocols & Standards, and advanced high speed buses.	2
3.4	Debugging methodologies	2
4	**Emulating SoC Architectures on FPGAs**	
4.1	Emphasis on different embedded processors and multiprocessor and architectures.	2
4.2	Coprocessor creation, hardware design for System-On-a-Chip.	2
4.3	Memory and peripheral interfacing.	2
4.4	System level design Tradeoffs, Power, Energy, Performance and Area.	2
5	**High level synthesis and system modeling**	
5.1	Exploration of HLS tools, System Modeling.	2
5.2	Models of Computation and System Specification Languages, High Level Computation/Behavioral Synthesis.	3
5.3	Application case study like FFT, JPEG.	3

Text Books

1. R. Sass and A. G. Schmidt. Embedded Systems Design with Platform FPGAs Principles and Practices. Elsevier Inc, USA, 2010.

2. The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Strathclyde Academic Media , UK ,2014.

Reference Books

1. S. Hauck and A. DeHon, Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing, Morgan Kaufmann, 2008.

2. Cardoso, João M. P.; Hübner, Michael (Eds.), Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, Springer, 2011.

COURSE CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222PEC100	MINI PROJECT	PROJECT	0	0	4	2

Mini project can help to strengthen the understanding of student's fundamentals through application of theoretical concepts and to boost their skills and widen the horizon of their thinking. The ultimate aim of an engineering student is to resolve a problem by applying theoretical knowledge. Doing more projects increases problem solving skills.

The introduction of mini projects ensures preparedness of students to undertake dissertation. Students should identify a topic of interest in consultation with PG Programme Coordinator that should lead to their dissertation/research project. Demonstrate the novelty of the project through the results and outputs.The progress of the mini project is evaluated based on three reviews, two interim reviews and a final review. A report is required at the end of the semester.

Evaluation Committee - Programme Coordinator, One Senior Professor and Guide.

Sl. No	Type of evaluations	Mark	Evaluation criteria
1	Interim evaluation 1	20	
2	Interim evaluation 2	20	
3	Final evaluation by a Committee	35	Will be evaluating the level of completion and demonstration of functionality/ specifications, clarity of presentation, oral examination, work knowledge and involvement
4	Report	15	the committee will be evaluating for the technical content, adequacy of references, templates followed and permitted plagiarism level(not more than 25%)
5	Supervisor/Guide	10	
	Total Marks	100	

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222LEC100	RECONFIGURABLE COMPUTING LAB	LABORATORY 2	0	0	2	1

Preamble: Recent advances in data analytics, machine learning, artificial intelligence, etc. technologies have made a leap in computational requirement. Hence, for implementing practical applications of those technologies, hardware acceleration is essential. Further, the advances in VLSI technology have given upswing to a fresh class of computer architectures which take advantage of application-level parallelism. These reconfigurable computers can be quickly customized at the hardware level to perform exactly the computation required in hardware, overcoming the fixed hardware configurations found in many contemporary microprocessors. This course, covers the state-of heart in reconfigurable computing both from a hardware and software perspective.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Build reconfigurable system using FPGAs
CO 2	Integrate a SoC and port on FPGA
CO 3	Perform partial reconfiguration for various applications using peripheral devices.
CO 4	Demonstrate an embedded system on FPGA using IP blocks.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	2	-	-
CO 2	1	1	-	3	2	-	-
CO 3	2	-	2	3	-	-	-
CO 4	1	-	2	3	-	-	-

Assessment Pattern

Bloom's Category	Continuous Evaluation
Apply	40
Analyse	20
Evaluate	20
Create	20

Mark distribution

Total Marks	CIE	ESE
100	100	-

Continuous Internal Evaluation Pattern: 100 Marks

The laboratory courses will be having only Continuous Internal Evaluation and carries 100 marks. Final assessment shall be done by two examiners; one examiner will be a senior faculty from the same department.

List of Experiments

Sl. No	CO Mapping	Practical Exercises (60 Hours)
1	CO1	SoC Integration using Processor Core
2	CO1,CO2	Interfacing AXI Peripheral -GPIO
3	CO1,CO2	Interfacing AXI peripheral-UART
4	CO1,CO2	Interrupt mechanisms
5	CO3,CO4	Programming SoC using C language
6	CO2,CO4	System debugging
7	CO3	Interfacing hardware accelerator core as AXI peripheral
8	CO3	Performance evaluation and calculation of acceleration factor
9	CO3,CO4	Co-processor interfacing – tightly and loosely coupled.

Reference Books

1. R. Sass and A. G. Schmidt. Embedded Systems Design with Platform FPGAs Principles and Practices. Elsevier Inc, USA, 2010.
2. The Zynq Book: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Strathclyde Academic Media , UK ,2014
3. S. Hauck and A. DeHon, Reconfigurable Computing: The Theory and Practice of FPGA-Based Computing, Morgan Kaufmann, 2008.
4. Cardoso, João M. P.; Hübner, Michael (Eds.), Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, Springer, 2011.

SEMESTER II

PROGRAM ELECTIVE III

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC066	HIGH SPEED DIGITAL SYSTEM DESIGN	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: High speed digital design techniques have become increasingly important in the electronic system design industries due to the high switching rise/fall times of logic devices. It focuses on creating designs that are less susceptible to signal integrity, power integrity, and EMI/EMC problems. The course provides the knowledge to tackle the problems related to high switching of logic devices. The course is structured in such a way that it delivers the fundamental knowledge to advanced techniques in high speed digital design.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn the fundamentals of high-speed digital design
CO 2	Design transmission lines for high-speed PCB.
CO 3	Understand how to perform efficient power distribution and minimize noise of high-speed IC switching logic.
CO 4	Learn signalling techniques**,** details for laying out differential signaling for impedance control, minimizing reflections, and controlling EMI.
CO 5	Understand how to control high-speed clock and properly layout the bus structures.
CO 6	Learn various clocking schemes and clock management for timing control.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	2	1	-	3	-	-	2
CO 2	-	-	-	-	1	2	-
CO 3	-	2	2	-	2	-	-
CO 4	-	-	3	-	2	3	-
CO 5	2	-	-	3	-	-	-
CO 6	3	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20

Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: XXXX	***Course Name: High Speed Digital Design***

Time : 2.5 Hours		Maximum : 60 Marks

	PART A (Answer all questions)	
1	With proper example, briefly explain the power calculations at different stages of a logic gate. Assume a TTL gate is loaded with a capacitive load of 50pf. Let delta V = 2.7 V and Tr is 2ns. Compute dI/dt.	5 marks
2.	Design a power distribution network for a peripherally bonded ASIC. Your chip is 15 x 15 mm in area and contains 1M gate equivalents. Each gate equivalent drives a 200 femto Farad load and switches on average every third cycle of a 100 MHz clock. What is the total power dissipation of your chip? Assuming a peak current to average current ratio of 4:1 how many metal layers do you need to distribute power so that the overall power supply fluctuation of a 2.5 V supply is +/-250mV.	5 marks
3.	With proper depiction, explain the operation of a tri state driver circuit.	5 marks
4.	Illustrate synchronizer failure and metastability problem in digital circuits.	5 marks
5	With proper depiction, briefly describe various clocking schemes in digital circuits.	5 marks

	PART B (Answer any one question from each module)	
6.	Assume a PCB is designed with two parallel traces A and B separated with a mutual capacitance of 0.4pF. The impedance of both traces are 50 Ohm. Assume 5V single ended signalling, and a signal raises from 1 V to 5 V in 80psec time in trace A. Derive the expression for cross talk and compute the same. Will it affect the signal propagation in trace B? Justify your answer.	7 marks

7.	Twenty CPUs are connected to a shared memory via 74HCT640 Bus transceiver. The backplane bus is implemented using 50 Ohm controlled impedance traces that are 10in long. The capacitances of backplane traces are 2pf/inch. Given the 9ns maximum propagation delay for each transceiver and bus frequency is 33MHz. Verify the design is fine or not by computing 1. Load capacitance, 2. Drive resistance 3.Rise time of the bus 4. Power dissipation. The manufacturer specifications for 74HCT640 Bus transceiver is C_{IO} = 10pf, V_{CC} = 4.5v ,V_{OH} = 3.84V,I_{out} = 6mA	7 marks
8.	Assume a CMOS inverter is powered by a 5V power source and the inverter is switching at 10MHz. The power supply wiring inductance is 164nH and the inverter load capacitance is 50pF. Assume the maximum rate of change of voltage is the drive voltage and the rise time of the inverter gate is 5nsec. 1. Draw the voltage and current waveforms at the o/p of the inverter. 2. Calculate the power supply noise.	7 marks
9.	With proper depiction illustrate differential signalling.	7 marks
10.	A digital designer designed a circuit and the circuits failed to meet setup and hold time violations. He increased the frequency of operation of the circuit without affecting the circuit performance. Will the circuit pass the timing requirements? Justify your answer with proper depiction and timing.	7 marks
11.	With proper depiction briefly describe the challenges in clock management for high speed circuits.	7 marks
12.	With proper depiction briefly describe a DLL based clock aligner.	7 marks

Syllabus

Module I: Introduction to high-speed digital design

Frequency, time and distance - Capacitance and inductance effects. High seed properties of logic gates. Wire modelling. Transmission lines.

Module II: Power distribution and noise

Power supply network-power management for high speed designs. Noise sources in digital system-power supply noise. Power supply isolation.

Module III: Signaling convention and circuits

Signaling modes, Signaling over various transmission mediums. Transmitter and receiver circuits.

Module IV: Timing convention and synchronisation

Timing fundamentals. Open loop and closed loop timing. Clocking schemes, clock domain transfer.

Module V: Clock distribution

Clock management for high speed designs, PLL and DLL based clock aligners, Closed loop clock distribution.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Introduction to high-speed digital design**	
1.1	Frequency, time and distance - Capacitance and inductance effects	2
1.2	High seed properties of logic gates	2
1.3	Wire modelling	2
1.4	Transmission lines	2
2	**Power distribution and noise**	
2.1	Power supply network-power management for high speed designs.	3
2.2	Noise sources in digital system-power supply noise.	3
2.3	Power supply isolation	2
3	**Signaling convention and circuits**	
3.1	Signaling modes	3
3.2	Signaling over various transmission mediums	3
3.3	Transmitter and receiver circuits	2

4	**Timing convention and synchronisation**	
4.1	Timing fundamentals	3
4.2	Open loop and closed loop timing	3
4.3	Clocking schemes, clock domain transfer	2
5	**Clock distribution**	
5.1	Clock management for high speed designs	3
5.2	PLL and DLL based clock aligners	3
5.3	Closed loop clock distribution	2

Text Books

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic by",3rd Edition, Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library, 2006.
2. William J Dally, John W. Poulton, "Digital Systems Engineering", Cambridge University Press 2012.

Reference Books

1. Stephen H. Hall, Garrett W. Hall, and James A. McCall "High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by", Wiley, 2007.
2. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006.
3. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC003	WIRELESS TECHNOLOGIES	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: This course introduces students to the fundamentals of wireless and mobile communication concepts. This subject is framed to set the required background in wireless communication. Being the backbone for all the IT based developments; Wireless Technology has seen tremendous growth in the past decade. There are new techniques and protocols emerging from time-to-time to cater the requirements of this rapidly growing area. The subject will cover from rf fundamentals to the topics like cellular, WiFi, WPN and WSN technologies. The treatment would look at current and upcoming wireless communications technologies for various wireless accesses.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Understand the different wireless technologies available today
CO 2	An understanding on the functioning of wireless communication systems and evolution of different wireless communication systems and standards.
CO 3	An ability to compare recent technologies used for wireless and Mobile communication
CO 4	An ability to explain the architecture, functioning, protocols, capabilities and application of various wireless communication networks
CO 5	An ability to evaluate design challenges, constraints and security issues associated with Ad-hoc wireless networks.
CO 6	An ability to explain the Wireless Sensor Networks and Wireless Personal Area Network Technologies

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

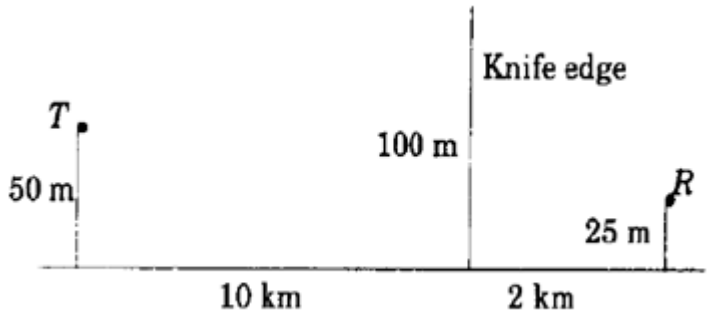
The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **222EEC003**	**Course Name: Wireless Technologies**

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		Discuss about InterSymbol Interference And how it can be resolved .	5 marks
2.		Discuss the working principle of *Software Defined Networking*.	5 marks
3.		From the following geometry, determine (a) loss due to knife edge refraction (b) height of obstacle to induce 6dB diffraction loss. Assume f=850MHz 	5 marks
4.		What are hidden node and exposed node problems; How can it be solved?	5 marks
5		Explain the main building blocks of Wireless Sensor Networks.	5 marks

		PART B (Answer any five questions)	
6		Discuss the OFDM technique in brief.	7 marks
7		Discuss the architecture of the GSM cellular system.	7 marks
8		Describe the difference Coherence time and coherence bandwidth	7 marks
9		Explain briefly about Wi-Fi Technologies and mention the Wireless	7 marks

		LAN requirements.	
10		Write a short note on *WiFi* Security standards.	7 marks
11		Explain Briefly about Bluetooth Technology and Profiles?	7 marks
12		Compare Zigbee, LoRa and Bluetooth Wireless Technologies.	7 marks

Syllabus

Wireless Communication Fundamentals - OFDM, MIMO - Cellular & Mobile technologies - Cellular Systems - Software Defined Networking (SDN) - Mobile Radio Propagation -Wireless Channel Models - Wireless LAN - *WiFi6, WiFi* Security standards - WSN and WPAN - Zigbee, Zwave, Thread, Bluetooth 1.0 to 6.0

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Wireless Communication Fundamentals**	
1.1	RF Basics: Radio Frequency (RF) Fundamentals: Introduction to RF & Wireless Communications Systems, Units of RF measurements, SNR, ISI	1
1.2	Analog& Digital Modulation techniques for Mobile communication,	2
1.3	Multiple access techniques	1
1.4	Wireless Antenna basics	1
1.5	OFDM, MIMO	2
2	**Cellular & Mobile technologies**	
2.1	The cellular concept - system design issues, Cellular carriers and Frequencies, Channel allocation, Cell coverage, Cell Splitting, Microcells, Picocells,	2
2.2	Handoff and outage, Improving coverage and system capacity	1
2.3	Cellular Systems (1G, 2G, 3G, 4G, 5G and beyond 5G)	2
2.4	NBIoT, Mobile IP	1
2.5	6G overview, Software Defined Networking (SDN) , Virtual RAN & Open RAN (VRAN & ORAN)	2
3	**Mobile Radio Propagation**	
3.1	Reflection, Diffraction. Fading.	1
3.2	Multipath Propagation.	3
3.3	Channel modeling, Diversity Schemes and Combining Techniques.	2
3.4	Wireless Channel Models	2
4	**Wireless LAN**	

4.1	Wi-Fi Organizations and Standards: Regulatory Bodies, IEEE, Wi-Fi Alliance,	1
4.2	WLAN Connectivity, WLAN QoS& Power-Save, IEEE 802.11 Standards,802.11-2007,802.11a/b/g, 802.11e/h/I,802.11n, 802.11AC.	1
4.3	Wi-Fi Hardware & Software: Access Points, WLAN Routers, WLAN Bridges, WLAN Repeaters	2
4.4	WLAN Controllers/Switches, Wireless Topologies	1
4.5	PoE Infrastructure, Wireless signaling.	1
4.6	WiFi6, WiFi Security standards	1
5	**WSN and WPAN**	
5.2	Wireless Sensor Network (WSN) & Wireless Personal Area Network(WPAN):	2
5.3	Introduction to WSN, WSN IEEE standards, WSN Topologies	2
5.4	WSN - Routing protocols, Low Power Lossy networks, RPL, TSCH and 6TiSCH	3
5.5	Zigbee, Zwave, Thread, Bluetooth 1.0 to 6.0, LoRA&LoRA WAN, WiMaX,6lowPAN,sigfox	3

Reference Books

1. Theodore S. Rappaport, "Wireless Communications: Principles and Practice", Second Edition, 2002, Pearson Education Asia.
2. David Tse and PramodViswanath, *Fundamentals of wireless communications*, Cambridge University Press, First Edition, 2012
3. Henrik Schulz And Christian L¨uders, *Theory and Applications of OFDM and CDMA Wideband Wireless Communications*, , John Wily & Sons, First Edition, 2005
4. Bluetooth Revealed; By: Miller, Brent A, Bisdikian, Chatschik; Addison Wesley Longman Pte Ltd., Delhi
5. Wilson , "Sensor Technology hand book," Elsevier publications 2005.
6. Andrea Goldsmith, "Wireless Communications," Cambridge University Press, 2005
7. Mobile and Personal Communications Services and Systems; 1 st Edition; By: Raj Pandya; PHI, New Delhi
8. Mobile Communications; By: Schiller, Jochen H; Addison Wesley Longman Pte Ltd., Delhi
9. 3G Networks: Architecture, protocols and procedures based on 3GPP specifications for UMTS WCDMA networks, By Kasera, Sumit, Narang, and Nishit, TATA MGH, New Delhi 8. Wireless Sensor Networks: information processing by approach, ZHAO, FENG, GUIBAS and LEONIDAS J, ELSEVIER, New Delhi 9. Holger Karl and Andreas Wiilig, "Protocols and Architectures for Wireless Sensor Networks" John Wiley & Sons Limited 2008
10. Wireless Communications and Networking,VijayGarg, Elsevier

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC005	FPGA BASED SYSTEM DESIGN	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: FPGA based system design covers the advanced design and emulation of digital circuits with Hardware Description Language (HDL) & with Field Programmable Gate Arrays (FPGA). The primary goal of this course is to provide in depth understanding of logic and system design. The course enables students to apply their knowledge for the modelling of advanced digital hardware systems for FPGA based prototyping.

Upon successful completion of this course, students will be able to:

Course Outcomes: After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of Design combinational and sequential digital circuits. (Cognitive knowledge level: **Understand**).
CO 2	Model digital circuits with Verilog HDL at behavioural, structural, and RTL Levels (Cognitive knowledge level: **Understand, apply and evaluate**).
CO 3	Develop test benches to simulate RTL designs (Cognitive knowledge levels: (Cognitive knowledge level: **Understand, apply and evaluate**).
CO 4	Develop RTL design of data path units and control units for microcomputer designs (Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 5	Understand in detail Programmable Logic fundamentals Cognitive knowledge levels: **Understand**).
CO 6	Understand in detail FPGA based prototyping flow.Cognitive knowledge levels: **Understand & Apply**).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1						1	
CO 2			2		3		
CO 3					2	2	
CO 4			2		3	2	
CO 5		1	2			3	
CO 6			2			2	

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation : 15 marks

Test paper, 1 number : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

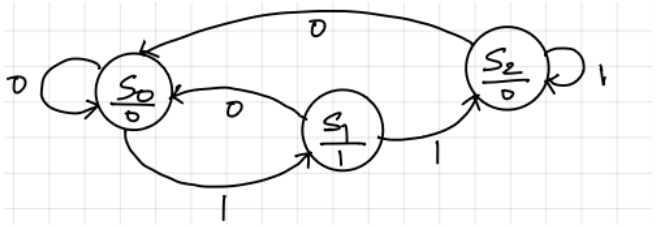
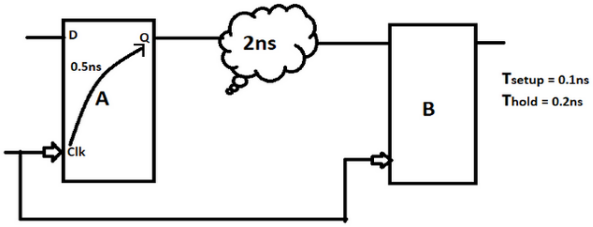
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: 222EEC005	***Course Name: FPGA BASED SYSTEM DESIGN***

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		Differentiate between tasks and functions in verilog	5 marks
2.		Write the verilog code for a D latch and a D flip flop. Evaluate the difference with the help of timing diagrams.	5 marks
3.		Explain briefly the significance of setup time and hold time in terms of design of digital circuits.	5 marks
4.		Describe about the concept of clock gating with the help of neat diagram.	5 marks
5		Draw and explain the logic blocks of FPGA	5 marks

		PART B (Answer any five questions)	
6.		Write a verilog program to implement 8:1 mux using 4:1 mux and 2:1 mux using hierarchical modelling	7 marks
7		Design a sequence detector that produces an output =1, when it receives a sequence of four consecutive ones (1111). Output 1 should be produced at the same time as the fourth input. At all other times, the output=0. After receiving the successful input sequence of 1111(which produces output=1), A new input sequence of 1111 must be received again to produce output=1 (That is , the successful input sequences of 1111 must be non-overlapping) Describe the FSM and verify the same with test bench. Example sequence: Input : 00011110100111100111111111110 Output: 00000010000000100000100010000	7 marks

8.		For the given FSM, illustrate the functionality with timing and write the verillog code for the circuit.  	7 marks
9.		Explain in detail the significance of timing concepts such as setup time, hold time and slack	7 marks
10.		Find the maximum frequency of operation. Given that T_{setup}=0.1ns, T_{hold}=0.2ns, T_{comb}=2ns, T_{pd}=0.5ns. What will happen if a positive skew of 3ns is added?  	7 marks
11.		Illustrate the design flow of FPGA with neat diagram	7 marks
12.		With proper depiction, explain FPGA based embedded system design.	7 marks

Syllabus

Introduction to Digital VLSI Design flow, Hardware modelling using Verilog HDL, Design abstractions, RTL design of digital subsystems, FSM coding, RTL design of data path and control units, Timing fundamentals, Advanced Timing concepts, FPGA architecture and design, Embedded Processor cores.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**HARDWARE MODELING USING VERILOG HDL**	
1.1	Evolution of digital design, digital VLSI design flow, Data Types and Lexical conventions.	2
1.2	Design abstractions.	3
1.3	Tasks & Functions.	2
2	**RTL DESIGN OF DIGITAL SUBSYSTEMS**	
2.1	FSM Coding, Mealy and Moore machines, FSM code development, Sequential Machine Design Examples.	3

2.2	Arithmetic Circuits: Adders, Subtractor & Multiplier.	3
2.3	RTL design of data path and control units	2
3	**TIMING FUNDAMENTALS**	
3.1	Basic Static Timing Analysis Concept, Setup Time, Hold Time, Slack. Jitter.	2
3.2	Clock Latencies, Clock Skew, Recovery and Removal Time.	3
3.3	Propagation Delay Calculations, Timing Paths, Timing	3
4	**ADVANCED TIMING CONCEPTS.**	
4.1	Timing models	3
4.2	Setup time and hold time violation checks	2
4.3	Clock Gating, STA VS DTA, Virtual Clock, Unateness, Timing constraints.	4
5	**FPGA ARCHITECTURE AND DESIGN METHODOLOGY**	
5.1	FPGA Architecture building blocks	3
5.2	FPGA based prototyping flow	3
5.3	Intellectual Property Cores Embedded Processor, Clock Managers, General-Purpose I/Os.	2

Reference Books

1. FPGA-Based System Design by Wayne Wolf, Prentice Hall.
2. Verilog HDL- A guide to Digital Design & Synthesis, Paperback by Samir Palnitkar, Pearson India.
3. FPGA Prototyping by Verilog Examples by Pong P. Chu, Wiley.
4. FPGAs: Fundamentals, Advanced Features, and Applications in Industrial Electronics, CRC Press.
5. Advanced FPGA Design: Architecture, Implementation, and Optimization by Steve Kilts, IEEE Press.
6. Embedded Core Design with FPGAs by Zainalabedin Navabi, McGraw Hill.
7. Advanced Digital System Design - A Practical Guide to Verilog Based FPGA and ASIC Implementation by Shirshendu Roy,Ane Books Pvt Ltd.
8. Computer Organization and Design RISC-V Edition: The Hardware Software Interface by David A. Patterson, John L. Henness, Morgan Kaufmann.
9. Digital Design by M. Morris R. Mano and Michael D. Ciletti., Person Education.
10. Digital Design by Frank, John Wiley and Sons Publishers.
11. Digital Computer Arithmetic Datapath Design Using Verilog HDL by James E. Stine, Spinger.
12. Digital Design Principles and Practices by John F. Wakerly, Pearson Education.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC001	INTERNET OF THINGS(IOT)	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: The digital space has witnessed major transformations in the last couple of years and as per industry experts would continue to evolve itself. The latest entrant to the digital space is the Internet of Things (IoT). IoT can also be defined as interplay for software, telecom and electronic hardware industry and promises to offer tremendous opportunities for many industries. The number of Internet-connected devices (12.5 billion) surpassed the number of human beings (7 billion) on the planet in 2011, and by 2020, Internet-connected devices are expected to number between 26 billion and 50 billion globally. Therefore, to leverage India's strength as a leader in the global service industry, this course will help students to become part of the IoT ecosystem in the country.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Explain the concept of IoT.
CO 2	Networking basics for IoT application development.
CO 3	Analyze various protocols for IoT.
CO 4	Design a PoC of an IoT system using various hardware platforms
CO 5	Apply data analytics and use cloud offerings related to IoT.
CO 6	Analyze applications of IoT in real time scenario

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: 222EEC001	***Course Name: Internet of Things***

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		Discuss the IoT system architecture and standards	5 marks
2.		Discuss the available indegenious RISC V based SoC solutions for prototyping the IoT node.	5 marks
3.		Briefly discuss MQTT protocol and its application in IoT.	5 marks
4.		Write a short note on IoT Security.	5 marks
5		What is TinyML? Discuss the significance of TinyML in IoT perspective.	5 marks

		PART B (Answer any five questions)	
6.		Discuss 6LoWPAN and its applications in IoT.	7 marks
7.		How to interface a sensor or actuator to an embedded hardware development board? discuss with reference to the IoT context.	7 marks
8		Compare the LoRa, LoRaWAN, sigfox and NB-IoT connectivity technologies.	7 marks
9		Discuss about Open and commercial Cloud solutions for IoT applications.	7 marks
10		Discuss about ARM Cortex Microcontroller Security and Root Security Services (RSS)	7 marks
11		Discuss the detailed procedure for designing an IoT based system for Smart vehicle status monitoring system, also mention the hardware, software, cloud and security concepts used in designing the complete system with relevant flow diagrams and figures.	7 marks
12		Discuss the detailed procedure for designing an IoT based system for Smart Irrigation systems. Mention the hardware, software, cloud and security concepts used in designing the complete system with relevant flow diagrams and figures.	7 marks

Syllabus

Overview of IoT - IoT hardware Platforms - IoT connectivity & Protocols - IoT Access Technologies: WiFi, Zigbee, Zwave, Bluetooth - Data analytics, Cloud and IoT Security - Apache web servers - JSON - IoT Case studies

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Overview of IoT**	
1.1	Introduction to the Internet of Things	1
1.2	IoT system architecture and standards	1
1.3	Networking Basics - TCP/IP	1
1.4	Networking Basics - IP addressing basics (IPV4 and IPV6)	2
1.5	Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks	2
2	**IoT hardware Platforms**	
2.1	IoT Design Methodology – Embedded computing logic – Microcontroller-System on Chips	1
2.2	Hardware platforms for prototyping IoT node- Arduino, Raspberry Pi, NodeMCU, ESP32, ARM Cortex Microcontrollers, IoT mote hardware platforms, Swadeshi RISC V based solutions	3
2.3	Interfacing sensors and actuators with hardware platforms	2
2.4	Developing IoT applications using Raspberry Pi with Python Programming.	2
3	**IoT connectivity & Protocols**	
3.1	IoT Access Technologies: WiFi, Zigbee, Zwave, Bluetooth,UWB, sub1GHz, LoRaWAN, Sigfox and NB-IoT	3
3.2	Topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and LoRaWAN	2
3.3	IoT application level protocols: MQTT, CoAP, XMPP, HTTP/Rest Services, WebSockets	3
4	**Data analytics, Cloud and IoT Security**	
4.1	No SQL Databases Vs SQL Databases	1
4.2	Apache web servers	1
4.3	JSON	1
4.4	Open and commercial Cloud solutions for IoT	2
4.5	Python Web Application Frameworks for IoT	1
4.6	IoT data visualisation tools	1
4.7	IoT Security - Need for encryption, standard encryption protocol, lightweight cryptography, Trust models for IoT	1
4.8	ARM Cortex Microcontroller Security, Root Security Services (RSS)	1

5	**IoT Case studies**	
5.1	Smart Lighting, Smart home	1
5.2	Smart Agriculture, Smart farming	1
5.3	IoT for health care & patient monitoring	1
5.4	Smart and Connected Cities	1
5.5	Building end-to-end smart applications with TinyML	4

Reference Books

1. David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, —IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, Cisco Press, 2017

2. Alessandro Bassi, Martin Bauer, Martin Fiedler, Thorsten Kramp, Rob van Kranenburg, Sebastian Lange, Stefan Meissner, "Enabling things to talk – Designing IoT solutions with the IoT Architecture Reference Model", Springer Open, 2016

3.VijayMadisetti , ArshdeepBahga, Adrian McEwen (Author), Hakim Cassimally "Internet of Things: A Hands-on-Approach" ArshdeepBahga& Vijay Madisetti, 2014.

4. Gian Marco Iodice, TinyML Cookbook: Combine artificial intelligence and ultra-low-power embedded devices to make the world smarter

5. Olivier Hersent, David Boswarthick, Omar Elloumi , —The Internet of Things – Key applications and Protocols, Wiley, 2012

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC110	INFORMATION SECURITY	PROGRAM ELECTIVE 4	3	0	0	3

Preamble: Information security, often referred to as InfoSec, refers to the processes and tools designed and deployed to protect sensitive business information from modification, disruption, destruction, and inspection. This course helps to understand and explain the risks faced by computer systems and networks, identify and analyze security problems in computer systems and networks, explain how standard security mechanisms work, develop security mechanisms to protect computer systems and networks, write programs that are more secure and use cryptography algorithms and protocols to achieve computer security.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn fundamentals of cryptography and its application to network security
CO 2	Understand network security threats, security services, and countermeasures.
CO 3	Understand vulnerability analysis of network security
CO 4	Acquire background on hash functions; authentication; firewalls; intrusion detection techniques
CO 5	Gain hands-on experience with programming and simulation techniques for security protocols
CO 6	Obtain background for original research in network security, especially wireless network and MANET security
C0 7	Understand the tradeoffs and criteria/concerns for security countermeasure development
CO 8	Apply methods for authentication, access control, intrusion detection and prevention
CO 9	Indentify and mitigate software security vulnerabilities in existing systems

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: 222EEC010	***Course Name: Information Security***

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		What is brute force attack?	5 marks
2.		What is One Time Pad?	5 marks
3.		Write a note on Secure Hash Algorithm.	5 marks
4.		Differentiate Salami attack and Man-in-the- middle attack	5 marks
5		How is Email Security achieved?	5 marks

		PART B (Answer any five questions)	
6.		Describe the principal threats to secrecy of passwords. What are two common techniques used to protect a password file? Explain.	7 marks
7.		Explain the steps followed in public key cryptography algorithms	7 marks
8.		Differentiate AES and DES Algorithms	7 marks
9.		During its lifetime, a typical virus goes through the four phases. Explain.	7 marks
13.		Discuss several software security concerns associated with writing safe program code	7 marks
11.		Explain Honeypots	7 marks
12.		Write a note on Design and Types of Firewalls	7 marks

Syllabus

Introduction to Information Security - Conventional Cryptographic Techniques - Symmetric and Asymmetric Cryptographic Techniques, Authentication and Digital Signatures - Program Security - Security in Networks

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Introduction to Information Security**	
1.1	Attacks	1
1.2	Vulnerability	1
1.3	Security Goals	2
1.4	Security Services and mechanisms	2
2	**Conventional Cryptographic Techniques**	
2.1	Conventional substitution and transposition ciphers	1
2.2	One-time Pad	1
2.3	Block cipher and Stream Cipher	2
2.4	Steganography	1
3	**Symmetric and AsymmetricCryptographic Techniques, Authentication and Digital Signatures**	
3.1	DES	1
3.2	AES	1
3.3	RSA algorithm	1
3.4	Use of Cryptography for authentication	2
3.5	Secure Hash function	2
3.6	Key management – Kerberos	2
4	**Program Security :**	
4.1	Nonmalicious Program errors	1
4.2	Buffer overflow	1
4.3	Incomplete mediation	1
4.4	Time-of-check to Time-of- use Errors	2
4.5	Viruses	1
4.6	Trapdoors	1
4.7	Salami attack, Man-in-the- middle attacks	1
4.8	Covert channels	1
5	**Security in Networks :**	
5.1	Threats in networks	1
5.2	Network Security Controls – Architecture, Encryption	2
5.3	Content Integrity, Strong Authentication, Access Controls	2
5.4	Wireless Security, Honeypots, Traffic flow security	2
5.5	Firewalls – Design and Types of Firewalls, Personal Firewalls	2
5.6	IDS, Email Security – PGP,S/MIME	2

Reference Books

1. Security in Computing, Fourth Edition, by Charles P. Pfleeger, Pearson Education

2. Cryptography And Network Security Principles And Practice, Fourth or Fifth Edition, William Stallings, Pearson

3. Modern Cryptography: Theory and Practice, by Wenbo Mao, Prentice Hall.

4. Network Security Essentials: Applications and Standards, by William Stallings. Prentice Hall.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC068	AUTOMOTIVE ELECTRONICS	PROGRAM ELECTIVE 3	3	0	0	3

Preamble: The objective of this Programme in Automotive Electronics is focused more on the design of modern electronic hardware systems for automotive applications. Emphasis is placed on a creative and imaginative approach to automotive electronics system design. Embedded Processor application for Engine controls, Power Train and Cruise Controls, Safety, Security and Comforts, Driveline & Axle, Motion, Stability and Chassis Control, Radio, Audio, Video and Navigation, Consumer to Automotive Interface

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn Vehicle Electronics Architecture (Cognitive knowledge level: Understand)
CO 2	Attain comprehensive understanding of various Block Hardware, Software, Component and Vehicle Interface (Cognitive knowledge level: Understand).
CO 3	Understand Fundamental Blocks Digital Communication Architecture, CAN Communication Node Architecture, CAN Protocol Controller (Cognitive knowledge levels: Understand, analyse, & create)
CO 4	Design Battery Switching Block, Ignition Start Sensing Block, Power Supply Block (Cognitive knowledge levels: Understand, analyse, create).
CO 5	Learn Vehicle EMC Compliance and Testing (Cognitive knowledge levels: Understand, analyse, create & Evaluate).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5
CO 1	3	-	-	-	-
CO 2	-	3	-	-	-
CO 3	2	-	-	-	3
CO 4	-	3	3	3	-
CO 5	-	-	-	-	3

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : **15 marks**

Course based task/Seminar/Data collection and interpretation: **15 marks**

Test paper, 1 number : **10 marks**

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SECOND SEMESTER M.TECH DEGREE EXAMINATION

Course Code: 222EEC068	**Automotive Electronics**

Time : 2Hr 30 minute		Maximum : 60 Marks

	PART A (Answer all questions)	
	Module I	
1	Which module is the most logical candidate to embed cruise control functions?	5 marks
	Module II	
2.	What are the types of microcontrollers used in automotive industry?	5 marks
	Module III	
3.	A vehicle is equipped with a total of 12 modules, 5 modules works only when the ignition switch is turned-on, however rest of the modules stay alive even if the ignition switch is turned-off. If each module is consuming 1.5 mA after the ignition switch has been turned-off, calculate the key-off load current (KOL)?	5 marks
	Module IV	
4.	What are the power delivery mechanisms?	5 marks
	Module V	
5	What are the critical noise factors in a typical vehicle that could impact module electronics?	5 marks

	PART B (Answer any five questions)	
	Module I	
6.	Modify the high level vehicle electronics architecture below by adding a power supply module feeding all modules from the vehicle battery. Show all the deletions and additions as necessary	7 marks
	Module II	

7.	Compare and contrast RISC verses CISC based architectures?	7 marks
	Module II	
8.	Why there is a need to have "switched-battery" controlled by the software?	7 marks
	Module III	
9.	The vehicle manufacturer has assigned a fuse with the intention of blowing the fuse if an overload occurs. Draw a fusing strategy diagram, showing the complete current path including the printed circuit board traces.	7 marks
	Module III	
10.	Draw a block diagram of a module showing switches and solenoids to control four (4) door-locks using FreeScale Star 12 processor. Also show the port assignment for the MS-CAN connectivity to other module?	7 marks
	Module IV	
11.	Explain Power Supply Module in Electric Vehicle	7 marks
	Module V	
12.	Draw Signal coupling chart	7 marks

Syllabus

Module-I Vehicle Electronics Architecture

Instrument Cluster, Heating and Cooling, Airbag Safety, Antilock Brake, Traction and Stability, Power Assist Steering, Automotive X- By-Wire, Tire Pressure Monitoring, Distributed Vehicle Architecture, Modules Cross Compatibility, Integrating Dissimilar Functions, Integrating Identical Functions, Microcontrollers Programming Options

Module-II Fundamental Module Blocks

Module Hardware Block - The Safety and Protection, The Switched Battery, The Ignition Switch, Start Interface, The Ignition Switch Run and Accessory Interface

Module Software Component - Application Software, Primary Boot Loader, The Real Time Operating System (RTOS), Network, Operating System (NOS)

Vehicle Interface - Vehicle Alternator, Relays and Solenoids, Battery, and Starter Motor, Vehicle Specific Input Functions, Vehicle Specific Output Functions, Diagnostics Connector, Service Tools, Secondary Boot loader

Module-III - Fundamental Blocks Topology

Safety and Protection, Power Supply, Battery Power Switching, Sensor Power Switching, Ignition Switch Interface, Digital Communication Architecture, CAN Communication Node Architecture, CAN Protocol Controller, Controller Area Network Transceiver, CAN Bus Implementation Strategies, CAN Bus Software Components, Battery Voltage Monitoring

Module-IV - Fundamental Blocks Design

Battery Switching Block, Ignition Start Sensing Block, Low-Side Output Device Driver, High-Side Output Device Driver, B+ Detection Block, B+ Monitoring Block, Input Signal Senor Block, Reset Block, Reverse Battery, Power Supply Block

Module-V - Module and Vehicle EMC Compliance

Automotive Radiated Emission, Automotive Conducted Emission, Automotive Radiated Immunity, Automotive Conducted Immunity, Automotive Radiated Emissions Testing, Automotive Conducted Emissions Testing, Testing RF Radiated Immunity Above 400–3,100 MHz, Testing Radiated Immunity Bulk Current Injection, Method, Cellular Phone Immunity Tests, Testing Automotive Conducted and Coupled Immunity, Immunity Tests Operational Classifications, Module Wire Coupling Tests, Module ESD Test, Module Conducted Immunity Tests

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module -I** Vehicle Electronics Architecture	
1.1	Automotive X- By-Wire	3
1.2	Communication Link	3
1.3	Microcontrollers Programming	2
2	**Module II -** Fundamental Module Blocks	
2.1	Module Hardware Block	3
2.2	Module Software Component	3
2.3	Vehicle Interface	2
3	**Module III -** Fundamental Blocks Topology	
3.1	Safety and Protection	3
3.2	Sensor Power Switching	3
3.3	Digital Communication Architecture	2
4	**Module IV -** Fundamental Blocks Design	
4.1	Battery Switching Block	3
4.2	Ignition Start Sensing Block	3
4.3	Sensors Power Switching Block	2
5	**Module V -** Module and Vehicle EMC Compliance	
5.1	Automotive Noise	3

5.2	Immunity Tests Operational Classifications	3
5.3	Module Conducted Immunity Tests	2

Text Books

1. Automotive Electronics Design Fundamentals, Najamuz Zaman, Springer

Reference Books

1. Automotive Electronics Handbook, Ronald K Jurgen, McGraw-Hill

2.Understanding Automotive Electronics: An Engineering Perspective, William Ribbens, Butterworth-Heinemann

SEMESTER II

PROGRAM ELECTIVE IV

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC069	EMBEDDED OS AND RTOS	PROGRAMME ELECTIVE 4	3	0	0	3

Preamble: Linux-based embedded systems are widely used in smartphones, in-vehicle infotainment systems, in countless consumer electronics and for numerous industrial applications. As a result, the demand for qualified embedded system engineers with the requisite experience in Linux is on the rise. This course teaches how to configure the Linux kernel and develop custom peripheral drivers. Learners gain an understanding of the Linux architecture, Real Time Operating System and acquire the practical skills involved in building an embedded os based system, as well as debugging and profiling application performance.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Attain comprehensive understanding of Embedded OS (Linux) fundamentals (Cognitive knowledge level: **Understand**).
CO 2	Attain comprehensive understanding of Embedded Processor and its software (Cognitive knowledge level: **Understand**).
CO 3	Attain comprehensive understanding of Embedded Linux Drivers (Cognitive knowledge levels: **Understand, analyse, &create**)
CO 4	Attain comprehensive understanding of basics of real-time concepts (Cognitive knowledge levels: **Understand, analyse, create and apply**)
CO 5	Attain comprehensive understanding of incorporating RTOS in an Embedded system(Cognitive knowledge levels: **Understand, analyse, create & Evaluate**).
CO 6	Attain comprehensive understanding of applying the knowledge for developing practical applications of modern real-time systems (Cognitive knowledge levels: **Understand & Apply**)

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	1	-	3	-	-	-
CO 2	-	-	-	-	1	2	-
CO 3	-	-	2	-	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	2	-	-	3	-	-	-
CO 6	2	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	20
Evaluate	10
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Micro project/Course based project : 20 marks
Course based task/Seminar/Quiz : 10 marks
Test paper, 1 no. : 10 marks
The project shall be done individually. Group projects not permitted. Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **222TEC001**	***Course Name: Embedded OS and RTOS***

Time : 2.5 Hours		Maximum : 60 Marks

	PART A (Answer all questions)	
1	Discuss about directory structure of Linux OS.	5 marks
2.	Discuss the difference between user space program and Kernel space program with the help of examples	5 marks
3.	Write a short note on qemu?	5 marks
4.	"Missing the deadline will be catastrophic". Analyze the context with respect to real time systems.	5 marks
5	How to assign priorities in Free RTOS? Explain how a multi-threaded application can be created with three different priorities?	5 marks

	PART B (Answer any five questions)	
6.	Write a multi-threaded C program in Linux whose main thread accepts multiple parameters of different types from the user and passes arguments to a thread and upon completion the thread returns values back to the main thread.	7 marks
7	Describe the procedure for developing a USB device driver in Linux.	7 marks
8	Discuss about how to customize Linux OS and the procedure to port OS to ARM based Embedded Target board.	7 marks
9	Explain the classification of real-time systems as Hard, Soft and Firm with suitable examples?	7 marks
10	Explain the different scheduling options available in RTOS?	7 marks
11	How to assign priorities in Free RTOS? Explain how a multi-threaded application can be created with three different priorities?	7 marks
12	Write a short note on different RTOS and its features used in Embedded real time applications.	7 marks

Syllabus

Module1: Introduction to Embedded Linux

Overview of Linux OS, Directory structures, basic Linux shell commands, Overview of Systems Calls, Classification of system Calls, Inter Process Communication, Multithreading and Thread Management

Module2: Embedded Linux Driver Development
Linux Kernel Module Programming, Character device driver development, USB device driver development, Block, Network and PCI device driver development

Module3: Building and Customisation of Linux for Embedded systems
Linux booting procedure, Bootloader, hypervisor, opensbi, qemu, Linux build tools - Buildroot and Yocto

Module4: Overview of Real Time OS
Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, RTOS Issues – Selecting a Real Time Operating System

Module5: RTOS for Embedded Applications
FreeRTOS, Thread creation & Management, Inter thread Communication, Mutual Exclusion, MbedOS, Other real time OS (VxWorks, Azure RTOS, SAFERTOS etc.)

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module1: Introduction to Embedded Linux**	
1.1	Overview of Linux OS, Directory structures, basic Linux shell commands	1
1.2	Overview of Systems Calls, Classification of system Calls	3
1.3	Inter Process Communication	2
1.4	Multithreading and Thread Management	3
2	**Module2: Embedded Linux Driver Development**	
2.1	Linux Kernel Module Programming	2
2.2	Character device driver development	3
2.3	USB device driver development	2
2.4	Block, Network and PCI device driver development	1
3	**Module3: Building and Customisation of Linux for Embedded systems**	
3.1	Linux booting procedure	3
3.2	Bootloader, hypervisor, opensbi	1
3.3	qemu	2
3.4	Linux build tools - Buildroot and Yocto	2

4	**Module4: Overview of Real Time OS**	
4.1	Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time	2
4.2	Differences between General Purpose OS & RTOS, Basic architecture of an RTOS	1
4.3	Scheduling Systems	2
4.4	RTOS Issues – Selecting a Real Time Operating System	1
5	**Module5: RTOS for Embedded Applications**	
5.2	FreeRTOS, Thread creation & Management, Inter thread Communication, Mutual Exclusion	4
5.3	MbedOS	2
5.4	Other real time OS (VxWorks, Azure RTOS, SAFERTOS etc.)	1

Reference Books

1. GNU/LINUX Application Programming, Jones, M Tims
2. Sreekrishnan Venkateswaran Essential Linux Device Drivers, Prentice Hall 2008
3. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK
4. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society
5. FreeRTOS Reference Manual

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC008	HARDWARE DESIGN VERIFICATION	PROGRAM ELECTIVE 4	3	0	0	3

Preamble: Design verification is the most important aspects of hardware development, consuming as much as 60 to 80 percentage of development time. The course covers the design verification methods for complex digital integrated circuits. The recent trend in the semiconductor industry is toward System on Chip (SoC) design and development for various applications. In a SoC usually, many processor cores and the essential peripherals are wrapped. The major skill sets required for a design verification engineer are knowledge of processor architectures, SoC verification flow, SoC subsystems, parallel bus architecture, knowledge of various peripheral intellectual property (IP) cores, and test environment integration. Furthermore, knowledge of a design and verification language, verification methodology, etc. are required for building the verification environment, writing test cases, and test integration. The course delivers the necessary skills (System Verilog-based verification, assertion-based, and coverage-driven verification, random verification, verification methodologies, etc.) required for design verification industry.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Create test benches for block-level verification
CO 2	Learn a hardware design verification language
CO 3	Develop automated test environment and test cases
CO 4	Understand complexities in SoC verification
CO 5	Perform methodology based verification of complex SoCs
CO 6	Perform coverage driven, constraint random and assertion based verification of complex designs.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	-	2	3	-	-	-
CO 2	1	-	-	-	2	-	-
CO 3	1	-	2	3	-	-	-
CO 4	-	-	2	-	-	-	-
CO 5	1	-	-	2	3	2	-
CO 6	-	-	2	3	2	2	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	10
Evaluate	10
Create	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **222EEC008**	***Course Name:*** **Hardware Design Verification**

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		What is an assertion? List the difference between concurrent and procedural assertions.	5 marks
2.		Why System Verilog interfaces are usually virtual. List the difference between normal interface and virtual interface.	5 marks
3.		Write functional coverage model to verify a mod 8 counter.	5 marks
4.		Assume a CPU is having 4 instructions {ADD,SUB,INC,DEC} , 4 registers{R0,R1,R2,R3} and 4 bit data, having 8 bit opcode. Write SV verification code to test the functionality of CPU. Use user defined data types to specify opcodes.	5 marks
5		Explain the need for the design verification methodology.	5 marks

		PART B (Answer any five questions)	
6.		Design an 8 bit counter, and write self-checking test bench to verify the design.	7 marks
7.		Design verification architecture for a 128 X 8 SRAM. Implement the same using Verilog HDL. Use tasks to obtain good code density.	7 marks
8.		With proper examples compare aggregation and inheritance property of SV class.	7 marks
9.		Develop System Verilog test bench to verify a 1024X8 Memory.	7 marks
10.		Design a ones counter with the following behavior. Ones Counter is a Counter which counts the number of one's coming in serial stream. The Minimum value of the count is "0" and count starts by incrementing one till "15". After "15" the counter rolls back to "0". Reset is also provided to reset the counter value to "0". Reset signal is active low. Input is 1 bit port for which the serial stream enters. Out bit is 4 bit port from where the count values can be taken. Reset and clock pins are also provided. Develop a System Verilog based test bench to verify the design.	7 marks

11.		With proper depiction, briefly explain the phases of an SoC verification.	7 marks
12.		Design a UVM test bench for an eight bit ALU.	7 marks

Syllabus

Module I: Overview of hardware design verification
Overview of Verilog HDL. Design Verification using Verilog HDL-types of test benches, writing test cases. Verification Architecture, Test automation. Assertions and Coverage.

Module II: Hardware Design Verification Language-System Verilog
Introduction to C/C++, Object orient programming. Overview of Verification language-System Verilog. System Verilog test benches. Functional verification.

Module III: System Verilog Advanced features
Coverage driven Verification-System Verilog functional coverage. Constraint Random Verification. Assertion based Verification. IP Verification a case study.

Module IV: SoC Verification
Overview of SoCs. SoC Verification architecture. Verification planning and phases of verification. Verification planning and phases of verification. Building SoC Verification environment. Writing test cases and test automation.

Module V: Methodology based Verification
Introduction to verification methodologies, Universal Verification Methodology (UVM), UVM components. Building UVM test bench/verification environment. UVM based IP verification a case study.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Overview of hardware design verification**	
1.1	Overview of Verilog HDL	2
1.2	Design Verification using Verilog HDL-types of test benches, writing test cases.	2
1.3	Verification Architecture, Test automation.	2
1.4	Assertions and Coverage.	2
2	**Hardware Design Verification Language-System Verilog**	
2.1	Introduction to C/C++, Object orient programming	2
2.2	Overview of Verification language-System Verilog	2
2.3	System Verilog test benches	2
2.4	Functional verification	2
3	**System Verilog Advanced features**	
3.1	Coverage driven Verification-System Verilog functional coverage	2
3.2	Constraint Random Verification	2

3.3	Assertion based Verification	2
3.4	IP Verification a case study	2
4	**SoC Verification**	
4.1	Overview of SoCs	2
4.2	SoC Verification architecture	2
4.3	Verification planning and phases of verification	2
4.4	Building SoC Verification environment. Writing test cases and test automation.	2
5	**Methodology based Verification**	
5.1	Introduction to verification methodologies	2
5.2	Universal Verification Methodology (UVM), UVM components	2
5.3	Building UVM test bench/verification environment.	2
5.4	UVM based IP verification a case study	2

Reference Books

1. Spear, C. and Tumbush, G. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features,3 rd Edition, Springer, 2012.
2. Design Verification with 'e': By Samir Palnitkar.
3. Hardware Design Verification: Simulation and Formal Method-Based Approaches: By William K. Lam, Prentice Hall
4. Writing Testbenches: Functional Verification of HDL Models: By Janick Bergeron, Springer

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC011	VLSI SIGNAL PROCESSING	PROGRAM ELECTIVE 4	3	0	0	3

Preamble: Digital signal processing (DSP) has emerged over the last two decades as the single most key component in all electronic applications, e.g., multimedia and mobile communications, video compression, digital still and network cameras, mobile phones, smart antennas, GPS, biomedical signal processing, etc. Most of these applications impose several challenges in the implementation of DSP systems, like the capability to process high throughput data as demanded by the real-time application, as well as requiring less power and less chip area. This course aims at providing comprehensive coverage of some of the important techniques for designing efficient VLSI architectures for DSP. The course covers the skill sets required for a DSP engineer to implement various signal processing algorithms efficiently on a hardware platform like FPGA.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	To cover techniques for designing efficient DSP architectures.
CO 2	To realize DSP architectures that will process high throughout data end/or require less power and / or less chip area.
CO 3	To learn a complete DSP system and fundamentals of pipelining and parallel processing.
CO 4	To study the concepts of retiming, unfolding, transforms and rank order filters.
CO 5	To study different bit level architectures and their complexities.
CO 6	To realize array signal processing structures like spatial filter.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	2	-	1	3	-	-	-
CO 2	-	-	2	-	3	2	-
CO 3	-	-	2	3	2	-	-
CO 4	-	-	3	-	2	-	-
CO 5	1	-	-	3	2	-	-
CO 6	-	-	-	3	-	-	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	10
Evaluate	10
Create	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

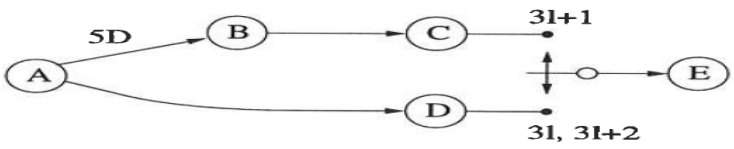
The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

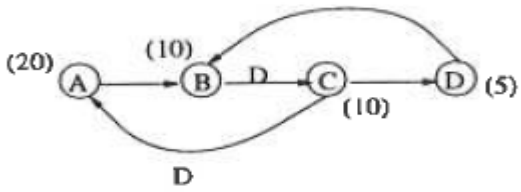
Model Question Paper

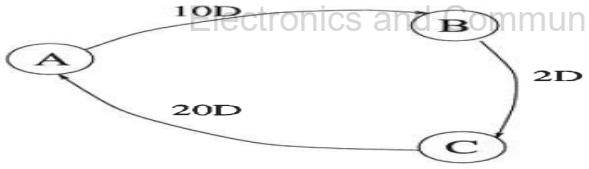
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **222EEC011**	***Course Name: VLSI Signal Processing***

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		Draw the systolic array structure of a 5 TAP FIR Filter.	5 marks
2.		Obtain a 2-parallel structure of the computation shown using unfolding transformation. 	5 marks
3.		Draw the structure and detail the RTL implementation of data broad cast 3 tap FIR filter.	5 marks
4.		Design a parallel pipelined architecture for radix-2 4-point FFT.	5 marks
5		Draw a coarse delay structure to obtain a maximum coarse delay of 200ns at a sampling frequency of 40MHz.	5 marks

		PART B (Answer any Five questions)	
6.		For the DFG shown, compute maximum sample rate and manually retime to minimize clock period. 	7 marks
7.		Unfold the DFG shown using Unfolding factors 3 and 4.	7 marks

			
8.		Illustrate with an example the pipelining of FIR digital filter.	7 marks
9.		Draw the structure and perform RTL implementation of the following equation. $y(n) = ax(n) + bx(n-2) + cx(n-5)$	7 marks
10.		Using Verilog HDL detail the RTL implementation of a 4-point parallel pipelined FFT architecture.	7 marks
11.		Draw the VLSI architecture of an 8 channel spatial filter.	7 marks
12.		Design a Delay line architecture to generate up to 1usec delay with 5ns resolution. Assume the sampling frequency is 40 MHz.	7 marks

Syllabus

Signal processing basics – DSP algorithms – Retiming – Folding and unfolding – DSP architectures – RTL design – RTL implementation – Filter implementation – FIR - IIR – DIT FFT – Array signal processing – Spatial Filters – DAS Filter

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Introduction to VLSI Signal processing**	
1.1	Graphical representation of DSP algorithms.	2
1.2	Dataflow and control flow	2
1.3	Parallel pipelined design of DSP Algorithms	2
1.4	Retiming	2
2	**Unfolding and Folding**	
2.1	Properties of unfolding	2
2.2	unfolding and retiming	2
2.3	Folding Transformation	2
2.4	Register Minimization Techniques	2
3	**VLSI Architectures for Digital Signal Processing**	
3.1	Architectural Design at Register Transfer Level	2
3.2	Design of data path and control path units	2
3.3	Verilog RTL implementation	4
4	**VLSI implementation of Filter and Transform structures**	
4.1	FIR and IIR architectures	4
4.2	Serial and parallel implementation of DIT-FFT algorithm.	4
5	**VLSI array signal processing**	

5.1	Overview of spatial filters	3
5.2	VLSI implementation of a delay and sum (DAS) spatial filter	5

Reference Books

1. VLSI Signal Processing Systems - Keshab K Parhi, John Wiley and Son's, NY 1999.

2. Architectures for Digital Signal Processing - Peter Prissch, John Wiley and Son's NY 1998.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC006	PRODUCT DESIGN AND QUALITY MANAGEMENT	PROGRAM ELECTIVE 4	3	0	0	3

Preamble: The course covers the 'foundation of product development processes. The course also covers quality management principles, techniques and tools associated with product development.

After successful completion of the course, students should be able to:

Demonstrate an ability to understand the product development process as adopted in industry; apply the tools and techniques for quality management in product development.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Attain good understanding of Product Design Fundamentals. (Cognitive knowledge level: **Understand**).
CO 2	Attain good understanding of Design for Manufacturing (DFM), Prototyping,(Cognitive knowledge level: **Understand, apply and evaluate**).
CO 3	Attain detailed understanding of Quality Management Principles & Techniques: (Cognitive knowledge level: **Understand, apply and evaluate**).
CO 4	Attain comprehensive understanding of Design of Experiments: **Understand, analyse, & Evaluate**).
CO 5	Attain good foundations of Design for Quality (Cognitive knowledge levels: **Understand, analyse, & Evaluate**).
CO 6	Understand in detail Six Sigma fundamentals, methods and tools: **Understand & Apply**).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1						1	
CO 2			2		3		
CO 3					2	2	
CO 4			2		3	2	
CO 5		1	2			3	
CO 6			2			2	

Assessment Pattern

Bloom's Category	End Semester Examination
Understand	20
Apply	30
Analyse	30
Evaluate	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation : 15 marks

Test paper, 1 number : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

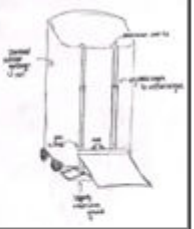
APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code:222EEC006	***Course Name:*** PRODUCT DESIGN AND QUALITY MANAGEMENT

Time : 2.5 Hours		Maximum : 60 Marks

		PART A (Answer all questions)	
1		Explain the steps in establishing product specifications	5 marks
2.		Explain with suitable example steps involved in managing product development projects.	5 marks
3		What is Signal to Noise Ratio Analysis in robust design? What are its advantages?	5 marks
4.		Analyse the possible causes for a 'Aero plane Crash' using a fishbone diagram.	5 marks
5		What is House of Quality? Explain with suitable depiction.	5 marks

		PART B (Answer any five questions)	
6.		Analyze which among the following designs (design 1 OR design 2) is the best from the given Pugh matrix(design selection matrix)	7 marks

Description		Standard Can	Collapsible Can	Can With Lift
Sketch				
Criteria	**Weight**	**Datum**	**Design 1**	**Design 2**
Durable	1	0	-	-
Portable	1	0	+	--
Affordable	2	0	0	--
Safe	3	0	0	--
Easy to Use	2	0	+	++

7.		Explain the different types of Intellectual Property rights applicable to products.	7 marks
8		Consider a medical equipment in a large hospital that is in use 16 hours a day, 7 days a week, measuring patients' heart signals. Over the last 6 months (26 weeks), the EKG machine has failed five times during normal operating hours, requiring downtime of four hours on each occasion to diagnose the issue and fix it. a.) Calculate Mean Time Between Failures (MTBF) b.) Failure rate	7 marks
9		Perform Failure Mode Effect Analysis for the given below possible failure modes of a cargo truck manufactured by a plant. a.) Head Lamp doesn't turn on b.) Headlamp doesn't turn off	7 marks
10		Consider two processes for PCB Manufacturing. Process X produces parts which have a mean width of 100 and a standard deviation of 2 .Process Y produces parts which have a mean width of 104 and standard deviation 3. The design specifications for the PCB are 100±10. Calculate: ● Cp for each process ● Cpk for each process And comment if the process is capable or not	7 marks
11		Illustrate the steps in Design for Six Sigma	7 marks
12		Explain the methodologies of Six Sigma	7 marks

Syllabus

Product design and development - Product architecture - Industrial design - Intellectual property Rights - Quality management principles and techniques - Design for quality: quality management tools - Six Sigma

Course Plan(For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**PRODUCT DESIGN AND DEVELOPMENT: I**	
1.1	Development processes, Identifying customer needs,	2
1.2	Establishing product specifications, Concept generation, Concept selection,	2
1.3	Product architecture, Industrial design.	3
2	**PRODUCT DESIGN AND DEVELOPMENT: II**	
2.1	Design for Manufacturing (DFM), Prototyping, Robust Design,	2
2.2	Intellectual property Rights	2
2.3	Product Development Economics, Managing Product Development Projects, Product Liability.	3
3	**QUALITY MANAGEMENT PRINCIPLES & TECHNIQUES**	
3.1	Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement, SPC, Quality Systems, Bench Marking	3
3.2	Frequency distributions and Histograms- Run charts –stem and leaf plots- Pareto diagrams-Cause and Effect diagrams-Box plots- Probability distribution-Statistical Process control	3
3.3	Scatter diagrams –Multivariable charts –Matrix plots and 3-D plots.-Reliability-Survival and Failure Series and parallel systems-Mean time between failure-Weibull distribution	3
4	**DESIGN FOR QUALITY: QUALITY MANAGEMENT TOOLS**	
4.1	Quality Function Deployment -House of Quality Design of Experiments –design process-Identification of control factors, noise factors, and performance metrics - developing the experimental plan	3
4.2	Process Capability and its index	2
4.3	Failure Mode Effect Analysis	2
5	**SIX SIGMA**	
5.1	Doctrine, Methodologies (DMAIC and DMADV)	2
5.2	Tools and Methods	3

5.3	Design for Six Sigma (DFSS)	3

Reference Books

1. Total Quality Management; by Dale H. Besterfield, Pearson Education Asia
2. Product Design & Development by Karl T Ulrich & Steven D Eppinger; McGraw Hill
3. Dieter, George E., "Engineering Design - A Materials and Processing Approach", McGraw Hill,
4. Product Design Techniques in Reverse Engineering and New Product Development, KEVIN
5. Product Design And Development, KARL T. ULRICH, STEVEN D. EPPINGER, TATA McGRAW-HILL- 3rd Edition, 2003.
6. The Management and control of Quality-6th edition-James R. Evens, William M Lindsay Pub:son
7. Fundamentals of Quality control and improvement 2nd edition, AMITAVA MITRA, Pearson Education

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC070	ELECTRIC VEHICLE TECHNOLOGY	PROGRAMME ELECTIVE 4	3	0	0	3

Preamble: The objective of this Programme in Electric Vehicle Technology is to make the students understand the principles behind the design of electric vehicles and the relevant technological and environmental issues. Students learn Modelling of Electric Vehicle, Electric Motor, Battery. How to design Motor control, Battery charging technique.

Course Outcomes: The COs shown are only indicative. For each course, there can be 4 to 6 COs.

After the completion of the course the student will be able to

CO 1	Learn EV Architecture and electric vehicle layout (Cognitive knowledge level: Understand)
CO 2	Attain comprehensive understanding of various Batteries, Battery Parameters, Battery Charging Technique (Cognitive knowledge level: Understand).
CO 3	Understand Fuel Cell Efficiency and Efficiency Limits (Cognitive knowledge levels: Understand, analyse, & create)
CO 4	Design Controller of Motor (Cognitive knowledge levels: Understand, analyse, create).
CO 5	Learn how to model the Acceleration of a Small Car (Cognitive knowledge levels: Understand, analyse, create & Evaluate).

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1	3	-	-	-	-	3
CO 2	-	3	-	-	-	-
CO 3	2	-	-	-	3	2
CO 4	-	3	3	3	-	-
CO 5	-	-	-	-	3	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	30
Analyse	30
Evaluate	30
Create	10

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2Hr 30 minute

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : **15 marks**

Course based task/Seminar/Data collection and interpretation: **15 marks**

Test paper, 1 number : **10 marks**

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 10 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

U	Slot **[SLOT]**
Reg. No:	Name:

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY

SECOND SEMESTER M.TECH DEGREE EXAMINATION

Subject: 222EEC070	**Electric Vehicle Technology**

Time : 2Hr 30 minute		Maximum : 60 Marks

	PART A (Answer all questions)	
	Module I	
1	Explain the operation of the Lithium Ion Battery	5 marks
	Module II	
2.	What are features of Inductive Power Transfer for Moving Vehicles?	5 marks
	Module III	
3.	Design a Simple edge connection of three cells in series	5 marks
	Module IV	
4.	Derive equation for induced torque and output torque for induction motor	5 marks
	Module V	
5	Derive equation for Rolling Resistance Force acting of vehicles	5 marks

	PART B (Answer any five questions)	
	Module I	
6.	How the hybrid vehicle layout are arranged and explain each module	7 marks

	Module II	
7.	Calculate Peukert Coefficient for batteries 42 Ah (10 h rating) and 33.6 Ah at a 1 h rating	7 marks
	Module II	
8.	What is the purpose of Modelling Battery?	7 marks
	Module III	
9.	Design production method of hydrogen fuel from Sodium Boro-hydride	7 marks
	Module III	
10.	Calculate the best possible efficiency in hydrogen production from Ammonia?	7 marks
	Module IV	
11.	A 460V 25hp 60Hz four pole Y connected induction motor has the following impedances in ohms per phase referred to the stator circuit R1=0.641ohm R2=0.332ohm X1=1.106ohm X2=0.464ohm Xm = 26.3ohm The total rotational losses are 1100W and are assumed to be constant. The core loss is lumped in with rotational losses. For a rotor slip of 2.2 percent at the rated voltage and rated frequency Find the motor's speed, stator current, power converter, power output?	7 marks
	Module V	
12.	Model the Acceleration of an Electric Scooter weigh 115kg and passenger weigh 70kg	7 marks

Syllabus

Module I - EV Architecture

Rechargeable battery electric vehicle layout, Hybrid vehicle layout, Parallel hybrid vehicle layout, Fuelled Evs, EVs which use Flywheels or Supercapacitors, Solar-Powered Vehicles, Principle of flywheel used as an energy store.

Module II - Batteries

Battery Parameters, Cell and Battery Voltages, Charge (or Amphour) Capacity, Energy Stored, Specific Energy, Energy Density, Specific Power, Amphour (or Charge) Efficiency, Energy Efficiency, Self-discharge Rates, Battery Temperature, Heating and Cooling Needs, Battery Life and Number of Deep Cycles, Batteries type, Battery Charging, Battery Modelling

Module III - Fuel Cells

Hydrogen Fuel Cells – Basic Principles, Different Electrolytes, Fuel Cell Electrodes, Fuel Cell Efficiency and Efficiency Limits, Efficiency and the Fuel Cell Voltage, Practical Fuel Cell Voltages, The Effect of Pressure and Gas Concentration, Connecting Cells in Series – The Bipolar Plate,Water Management in the PEMFC, Keeping the PEM Hydrated, Thermal Management of the PEMFC, A Complete Fuel Cell System

Module IV - Electric Machines and their Controllers

Brushed DC Electric Motor, Torque Speed Characteristics, Controlling the Brushed DC Motor, DC Motor Efficiency, Motor Losses and Motor Size, Electric Motors as Brakes, Regenerative braking of a DC motor, DC Regulation and Voltage Conversion, Step-Down or Buck Regulators, Step-Up or Boost Switching Regulator, Single-Phase Inverters, Three Phase Inverters, Brushless Electric Motors, Brushless DC Motor control, Switched Reluctance Motors, Induction Motor, Motor Cooling, Efficiency, Size and Mass

Module V - Electric Vehicle Modelling

Tractive Effort, Rolling Resistance Force, Aerodynamic Drag, Hill Climbing Force, Acceleration Force, Total Tractive Effort, Modelling Vehicle Acceleration, Acceleration Performance Parameters, Modelling the Acceleration of an Electric Scooter, Modelling the Acceleration of a Small Car

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	**Module -I EV Architecture**	
1.1	Battery Electric Vehicles	3
1.2	EVs which use Flywheels or Supercapacitors	3
1.3	Solar-Powered Vehicles	2
2	**Module II - Batteries**	
2.1	Battery Parameters	3
2.2	Battery Charging	3

2.3	Battery Modelling	2
3	**Module III - Fuel Cells**	
3.1	Hydrogen Fuel Cells	3
3.2	Water Management in the PEMFC	3
3.3	Thermal Management of the PEMFC	2
4	**Module IV - Electric Machines and their Controllers**	
4.1	Electric Motor Characteristics	3
4.2	DC Regulation and Voltage Conversion	3
4.3	Motor Cooling, Efficiency, Size and Mass	2
5	**Module V - Electric Vehicle Modelling**	
5.1	Tractive Effort	3
5.2	Modelling Vehicle Acceleration	3
5.3	Modelling Electric Vehicle Range	2

Text Books

1. Electric Vehicle Technology Explained, James Larminie John Lowry, Second Edition A John Wiley & Sons, Ltd., Publication

Reference Books

1. Handbook of Automotive Power Electronics and Motor Drives, Ali Emadi, CRC Press.

2. Advanced Electric Drive Vehicles, Ali Emadi, CRC Press.

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC009	MIXED SIGNAL SYSTEM DESIGN	PROGRAM ELECTIVE 4	3	0	0	3

Preamble: This course focuses on the concepts of mixed-signal system design. The course delivers the practical aspect of analog, digital and mixed-signal sub blocks of an electronic system. The course covers the fundamental principles of designing analog, mixed-signal, digital sub-blocks, and system integration. In addition, the course details the fundamentals of data converters, the central concept of oversampling, and noise shaping. As part of this course, candidates will use industry-standard tools for mixed-signal system design and simulation. The course is intended for candidates who are seeking to learn the mixed-signal circuit and system design.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Detailed knowledge of static and dynamic behaviour of CMOS logic.
CO 2	Basic understanding of Analog circuit building blocks
CO 3	Detailed understanding of CMOS Digital Subsystem Design.
CO 4	Detailed understanding of Analog Mixed Signal Circuit Design.
CO 5	To address practical issues in Analog Mixed Signal System Design.
CO 6	Detailed Understanding of Data Converters and practical design issues.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	1	-	-	3	-	-	-
CO 2	1	-	-	-	3	-	-
CO 3	1	-	2	3	2	-	-
CO 4	-	-	2	-	2	2	-
CO 5	1	-	-	2	3	-	-
CO 6	-	-	2	3	-	2	-

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	10
Evaluate	10
Create	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern: 40 Marks

Preparing a review article based on peer reviewed original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Data collection and interpretation: 15 marks

Test paper, 1 no. : 10 marks Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern: 60 Marks

The end semester examination will be conducted by the respective College. There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
MONTH & YEAR

Course Code: **222EEC009**	***Course Name:*** **Mixed Signal System Design**

Time : 2.5 Hours	Maximum : 60 Marks

		PART A (Answer all questions)	
1		Show that MOSFET acts as a controlled resistor in deep triode region.	5 marks
2.		With proper depiction briefly describe the implementation of a flip-flop using pass transistors.	5 marks
3.		Sketch and explain the working of a differential amplifier with passive load.	5 marks
4.		Briefly describe the interfacing of an ADC with a microcontroller.	5 marks
5		Detail the practical considerations while designing a mixed signal PCB.	5 marks
		PART B (Answer any Five questions)	
6.		Explain the formation of the transfer characteristic of CMOS inverter with a neat diagram.	7 marks
7.		Discuss the various short channel effects in MOS devices.	7 marks
8.		Implement the equation $X = ((\bar{A} + B)(\bar{C} + \bar{D} + \bar{E}) + \bar{F})\bar{G}$ using CMOS. Size the devices so that the output resistance is the same as that of an inverter with an NMOS W/L = 2 and PMOS W/L = 6.	7 marks
9.		With proper depiction, briefly describe the SNR analysis in the analog frontend signal chain of an electronic system.	7 marks
10.		Describe how the small-signal voltage gain of a differential amplifier can be computed by applying: (i) Principle of superposition, and (ii) concepts of virtual ground and half circuit.	7 marks
11.		Briefly describe the working principle of a pipe-lined ADC.	7 marks
12.		Detail the steps involved in bring-up of a mixed signal electronic system.	7 marks

Syllabus

Module I: Overview of mixed signal system design
MOS Transistor operation and circuit design. CMOS Inverter AC and DC Characteristics. Analog Signal Processing. Overview of Analog Mixed Signal Circuit Design.

Module II: Digital sub circuits
Fundamentals of CMOS logic implementation. Design and implementation of basic digital circuits-Flip-Flops, multiplexers, demultiplexers, encoders, decoders, etc. Design and implementation of complex digital sub-circuits-ALU, control unit, comparator, timer, PWM, etc. Design of memory subsystem.

Module III: Analog Sub circuits
Operational amplifier basics, Differential amplifier basics. Feedback concepts and design of VCO, PLL. Design of analog frontend sub blocks and signal chain analysis.

Module IV: Data converters
ADCs and DACs. Oversampling data converters.

Module V: Mixed Signal system design
High level and low level design of mixed-signal system. Practical considerations of mixed-signal PCB design. Mixed-signal system bring up.

Course Plan (For 3 credit courses, the content can be for 40 hrs and for 2 credit courses, the content can be for 26 hrs. The audit course in third semester can have content for 30 hours).

No	Topic	No. of Lectures
1	Overview of mixed signal system design	
1.1	MOS Transistor operation and circuit design	2
1.2	CMOS Inverter AC and DC Characteristics	2
1.3	Analog Signal Processing	2
1.4	Overview of Analog Mixed Signal Circuit Design	2
2	Digital sub circuits	
2.1	Fundamentals of CMOS logic implementation	2
2.2	Design and implementation of basic digital circuits-Flip-Flops, multiplexers, demultiplexers, encoders, decoders, etc.	2
2.3	Design and implementation of complex digital sub-circuits-ALU, control unit, comparator, timer, PWM, etc.	2
2.4	Design of memory subsystem	2
3	Analog Sub circuits	
3.1	Operational amplifier basics	2
3.2	Differential amplifier basics. Feedback concepts and design of	2

	VCO, PLL.	
3.3	Design of analog frontend sub blocks and signal chain analysis.	4
4	Data converters	
4.1	ADCs and DACs	4
4.2	Oversampling data converters	4
5	Mixed Signal system design a case study	
5.1	High level and low level design of mixed-signal system	2
5.2	Practical considerations of mixed-signal PCB design	4
5.3	Mixed-signal system bring up	2

Reference Books

1. CMOS Analog Circuit Design, 2nd edition; by: Allen, Phillip E, Holberg , Douglas R, Oxford University Press, (Indian Edition
2. D A John, Ken Martin, Analog Integrated Circuit Design, 1st Edition, John Wiley
3. Ken Martin, Digital Integrated Circuit Design, John Wiley
4. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3 rd edition, John Wiley & Sons.
5. Sedra & Smith, Microelectronics Circuits, 5th Edition, Oxford University Press, (Indian Edition)
6. Jan M. Rabaey, Anantha Chadrakasan, B. Nikolic ,Digital Integrated Circuits – A Design Perspective 2nd Edition, Prentice Hall of India (Eastern Economy Edition). 85 /104
7. Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design,2nd Ed, Tata McGraw Hill.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

SEMESTER II

INTERDISCIPLINARY ELECTIVE

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC084	MEMS AND SENSORS	INTERDISCIPLINARY ELECTIVE	3	0	0	3

Course Objectives

- Introduces students to the need of rapidly emerging, area of MEMSand microsystem in engineeringand its applications in sensor technology
- Enable the students to understand the various sensing and actuation mechanisms.

Prerequisite: nil

Course Outcomes: After the completion of the course the student will be able to

CO1	Identify structural and sacrificial materials for MEMS
CO2	Describe the fabrication steps in designing of various MEMS devices.
CO3	Apply principles for the design of Sensor and actuators
CO4	Apply MEMS for different applications in various fields of engineering

CO - PO MAPPING

CO	PO1	PO2	PO3	PO4	*PO5*
CO1					
CO2					
CO3					
CO4					

Assessment Pattern

Bloom'sCategory	Continuous Assessment Tests		End Semester Examination [%] (60Marks)
		Test1 [%] (10Marks)	
Remember		10	20
Understand		20	40
Apply		10	20
Analyse		10	20
Evaluate			
Create			

Mark distribution

Total Marks	CIE (Marks)	ESE (Marks)	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation: 40 marks

Preparing a review article based on peer reviewed Original publications (minimum 10 publications shall be referred) : 15 marks

Course based task/Seminar/Micro project : 15 marks

Test paper 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination: 60 marks

The end semester examination will be conducted by the respective college.

There will be two parts; Part A and Part B. Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions. Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

SYLLABUS

1	**MODULE I**

Introduction: Introduction to MEMS and Microsystems, MEMS Classification, MEMS versus Microelectronics, Applications of MEMS in Various Industries, Some Examples of Microsensors, Microactuators, and Microsystems, Materials for MEMS, Laws of Scaling in miniaturization

2	**MODULE II**

MEMS Fabrication: Structure of Silicon, Single Crystal Growth Techniques, Photolithography, Oxidation, Diffusion, Ion Implantation, Physical Vapor Deposition, Chemical Vapor Deposition, Bulk Micromachining: Overview of Etching, Isotropic and Anisotropic Etching, Wet Etchants, Etch Stop Techniques, Dry Etching, Surface Micromachining, LIGA, SLIGA, Wafer Bonding, Electroplating

3	**MODULE III**

Microsensors and Microactuators: Basic Modeling Elements in Mechanical, Electrical and Thermal Systems, Types of Beams: Cantilevers, Bridges, Fixed-Guided beams, Electrostatic sensing and Actuation: Parallel plate capacitor, Applications of parallel plate capacitors: Inertial sensor, Pressure sensor, Flow sensor, Parallel plate Actuators, Piezoresistive Sensors: Origin and Expressions of Piezoresistivity, Piezoresistive Sensor Materials, Applications of Piezoresistive Sensors, Piezoelectric Sensing and Actuation, Thermal Sensing and Actuation: Sensors and Actuators based on Thermal Expansion, Thermocouples, Thermoresistors, Shape Memory Alloy, Applications: Inertial sensors, Flow sensors, Infrared sensors

4	**MODULE IV**

Layout, Simulation Tools, Packaging and Characterization techniques: Introduction of layout, Simulation Tools, General considerations in Packaging , Bonding techniques for MEMS and Various Characterization Techniques for MEMS Devices

5	**MODULE V**

Advances in MEMS:RF-MEMS: MEMS devices for RF Applications: RF MEMS Switches and their applications, High-Q Capacitors and Inductors and Their

Applications in RF Circuits, Overview of Optical MEMS , Chemical-Bio MEMS and Nanoelectromechanical Systems

Text books

- MEMS and Microsystems design and manufacture by Tai-Ran Hsu, Tata McGraw Hill.
- MEMS by N. P. Mahalik, Tata McGraw Hill.
- Foundations of MEMS by Chang Liu, Pearson Prentice Hall.

Reference books

- Sensors and Transducers by M. J. Usher, McMillian Hampshire.
- Analysis and Design Principles of MEMS Devices by Minhang Bao, Elsevier.
- Fundamentals of Microfabrication by M. Madou, CRC Press.
- Microsensors by R.S. Muller, Howe, Senturia and Smith, IEEE Press.
- Semiconductor Sensors by S. M. Sze, Willy Inderscience Publications.

COURSE CONTENTS AND LECTURE SCHEDULE

No.		No. of Hours
	MODULE 1	
1.1	Introduction to MEMS and Microsystems, MEMS Classification, MEMS versus Microelectronics,	1
1.2	Applications of MEMS in Various Industries, Some Examples of Microsensors, Microactuators, and Microsystems	1
1.3	Materials for MEMS,	2
1.4	Laws of Scaling in miniaturization	1
	MODULE II	
2.1	Structure of Silicon, Single Crystal Growth Techniques,	1
2.2	Photolithography, Oxidation,	1
2.3	Diffusion, Ion Implantation,	1
2.4	Physical Vapor Deposition, Chemical Vapor Deposition,	1
2.5	Bulk Micromachining: Overview of Etching, Isotropic and Anisotropic Etching,	1
2.6	Wet Etchants, Etch Stop Techniques, Dry Etching	1

2.7	Surface Micromachining	1
2.8	LIGA, SLIGA	2
2.9	Wafer Bonding, Electroplating	1
MODULEIII		
3.1	Microsensors and Microactuators: Basic Modeling Elements in Mechanical, Electrical and Thermal Systems,	1
3.2	Types of Beams: Fixed-Free (Cantilevers), Fixed-Fixed (Bridges), Fixed-Guided beams,	1
3.3	Electrostatic sensing and Actuation: Parallel plate capacitor,	1
3.4	Applications of parallel plate capacitors: Inertial sensor,	1
3.5	Pressure sensor, Flow sensor, Parallel plate Actuators,	1
3.6	Piezoresistive Sensors: Origin and Expressions of Piezoresistivity, Piezoresistive Sensor Materials,	1
3.7	Applications of Piezoresistive Sensors,	1
3.8	Piezoelectric Sensing and Actuation,	1
3.9	Thermal Sensing and Actuation: Sensors and Actuators based on Thermal Expansion,	1
3.10	Thermocouples, Thermoresistors,	1
3.11	Shape Memory Alloy, Applications: Inertial sensors, Flow sensors, Infrared sensors	2
MODULEIV		
4.1	Introduction of layout, Simulation Tools,	1
4.2	General considerations in Packaging and bonding techniques in MEMS	2
4.3	Various Characterization Techniques for MEMS Devices	1
MODULEV		
5.1	Advances in MEMS: RF-MEMS: MEMS devices for RF Applications:	1
5.2	RF MEMS Switches and their applications,	1

5.3	High-Q Capacitors and Inductors and Their Applications in RF Circuits,	1
5.4	Overview of Optical MEMS ,	1
5.5	Chemical-Bio MEMS and Nanoelectromechanical Systems	1

Model Question Paper

A P J Abdul Kalam Technological University
Second Semester M.Tech Degree Examination
Course: 222EEC084MEMS and Sensors
Time: 150 Minutes Max. Marks: 60

PART A
Answer All Questions

1	Mention the criteria for selecting materials for the masks used in etching. List four materials used as masks.	5
2	Define etch stop? List different methods used to stop etching and explain one with sketches	5
3	Explain with neat sketches the type of mechanical beams and boundary conditions associated with supports	5
4	State the various levels of micro system packaging	5
5	With neat sketches explain the construction and working of a shunt type RF MEMS switch.	5

PART B
Answer any five question

6	A silicon substrate is doped with phosphorus ions at 100 KeV. Assume the maximum concentration after the doping is 30 x $10^{18}/cm^3$. Find: (a) the dose, Q, (b) the dopant concentration at the depth 0.15 μm, (c) the depth at which the dopant concentration is at 0.15% of the maximum value. (Given: Rp = 135 nm and ΔRp = 53.5 x 10^{-7}cm at 100 KeV energy level).	*7*
7	Explain in the light of scaling, assuming a 10 times reduction of size of the actuator. Which of the electrostatic and electromagnetic forces are best suited for micro device actuation and why?	*7*
8	Explain the purpose of micro cantilevers in MEMS systems. What is the relevance of Spring constant (k) of the mechanical structure in the microsystems.	*7*

9	Explain the principle of operation of the following micro sensors (i) Comb drives (ii) Shape Memory Alloys	*7*
10	Explain the challenges involved in BioMEMS. List three applications of BioMEMS.	*7*
11	Explain Various bonding techniques associated with MEMS and their implications on packaging	*7*
12	Explain the LIGA process associated with MEMS fabrication with suitable sketches	*7*

CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEC085	NANO MATERIALS FOR DRUG DELIVERY	INTERDISCIPLINARY ELECTIVE	3	0	0	3

Preamble: To inspire the students with interest to investigate role of new nanomaterials and devices drug delivery.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Familiarize the concepts of nano materials for drug delivery
CO 2	Investigate the use of nano materials for drug delivery
CO 3	Investigate the use of nanodevices for drug targeting

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6
CO 1			3			
CO 2			3			
CO 3			3			

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	20
Analyse	40
Evaluate	
Create	

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern

Micro project/Course based project : 20 marks
Course based task/Seminar/Quiz : 10 marks
Test paper, 1 no. : 10 marks
The project shall be done individually. Group projects not permitted. Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

There will be two parts; Part A and Part B. Part A will contain 5 short answer questions with 1 question from each module, having 5 marks for each question. Students should answer all questions. Part B will contain 7 questions with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Syllabus and course plan

No	Topic	No. of Lectures
1	**Nanomedicines**	
1.1	Basic concepts in the design, specification and desired features of nanomedicine and general process steps involved in their preparation Nanomedicines for various disease conditions: infectious diseases, neurological diseases, pulmonary disorders, cardiovascular diseases	4
1.2	cancer: nano-chemotherapy, - radiation therapy, - immunotherapy, -nuclear medicine therapy, -photodynamic therapy, - photothermal and RF hyperthermia therapy, scintillation therapy, gene-therapy: DNA, RNA delivery. Theranostic nanomedicines: Basic concept, multifunctional nanomedicines for theranosis	4
2	**Drug Delivery Systems**	
2.1	Administration Routes: Oral Drug Delivery, Features of Gastrointestinal tract (GI), Targeting of drugs in the GI tract.	4
2.2	Design and fabrication of oral systems - Dissolution controlled, diffusion controlled, osmotic controlled, chemically controlled release, Intravenous Drug Delivery - Factors controlling pharmacokinetics of IV formulations, Concept of opsonization	4
3	**Drug Delivery Devices**	
3.1	Transdermal Drug Delivery, Structure of human skin and theoretical advantages of the transdermal route, Transdermal penetration of drugs, adhesion, bioactivity.	4
3.2	Intranasal Drug Delivery - Nasal physiology and intranasal Drug Administration, Nasal drug delivery devices, Ocular Drug Delivery devices; Miscellaneous Drug Delivery	4
4	**Advanced Drug Delivery**	
4.1	Concept of Drug Targeting; Prodrug and Bioconjugation; Nanoscale Drug Delivery Systems - Advantages of nanodrug delivery – Improvements in pharmacokinetics, bioavailability, biodistribution; Concepts of controlled and sustained drug delivery, How nanoparticles pass barriers; Surface modification of nanoparticulate carriers	4

4.2	Nanocarriers for drug delivery - Lipid based pharmaceutical nanoparticles – Liposomes, Solid Lipid Nanoparticles, Nanostructured Lipid Carriers, Cubosomes and Hexosomes, Polymeric Micelles, DNA- Based Nanomaterials, Dendrimers, Polymeric nanoparticles, Inorganic nanoparticles, Hydrogels for controlled drug delivery	4
5	**Active and passive nanocarriers**	
5.1	Concept of targeting, Site Specific Drug delivery utilizing Monoclonal Antibodies, Peptides, Other Biomolecules, Stimuli-Responsive Target Strategies; Implants; Protein and Peptide Drug Delivery; Delivery of Nucleic Acids	3
5.2	Delivery of Vaccines; Aptamers in Advanced Drug Delivery; Biomimetic Self-Assembling Nanoparticles	2
5.3	Nanotechnology Challenges; Regulatory Considerations and Clinical Issues in Advanced Drug Delivery	3

Books-

1. Drug Delivery Systems, Pieter Stroeve and MortezaMahmoudi, World Scientific Series: From
2. Biomaterials towards Medical Devices, Vol I, 2018.
3. Nanoparticulates as Drug Carriers, Vladimir Torchillin, Imperial College Press, 2006
4. Drug Delivery Systems, Third Edition, Vasant V Ranade, John B. Cannon, by CRC Press, 2011