Course Description:

This is an online, instructor – led course which provides a thorough knowledge about the FPGA Hardware, its programming and interfacing. Two Weeks online training with Remote FPGA Lab Access for the candidates. Well Experienced Faculties from National Institute Technology, Meghalaya– (NIT Meghalaya) and National Institute of Electronics and Information Technology- (NIELIT Calicut) will be handling the sessions for all the 10 Days.

Program Objectives

To learn, Practice- FPGA Design Flow, Basics of Programming, Interfacing FPGA with ARM Processor for DSP Applications. To get exposure in industry standard methodologies.

Who can attend?

Students of Engineering (UG & PG) & MSc (Electronics), PhD scholars, faculty members and professionals from Industry.

- Proposed length of the training: 10 Days. 20 Hours lecture 30 Hours practicals.

Course Fee	
INR 3,000/- For Students INR 5,000/- For Faculty INR 8,000/- For Industry/Corporate Last date for payment and confirmation: 7-May-2021	**REGISTER NOW**

Payment Guidelines: -

Online fund transfer can be made via your Internet Banking, Google Pay to the following account and proof of the same has to be uploaded during the registration.

Account details:

Name of the Institute: National Institute of Electronics and Information Technology, Calicut.
Account Holder: Director NIELIT Calicut

Account No: 10401158037   **Bank Name:** SBI, NIT Chathamangalam

IFSC No: SBIN0002207   **MICR Code:** 673002012

For any queries WhatsApp to 9447769756, Please don't call, we will reply to you at the earliest.

Delivery Mode: Online. Live classes followed by online assignments over LMS. Students should have Laptop/PC with high speed internet connectivity.

Tentative Schedule

Duration		2 weeks
Tentative Timings		10 am to 12.00 noon (Theory) Lab/Assignments can be submitted online on Leaning management Systems (Any Time)
Tentative dates		10th May 2021

		Syllabus		
		Theory	LAB	Faculty (Indicative)
Day 1		Verilog HDL-1	Mentor Graphics or Xilinx Vivado Simulation	NIELIT Calicut
Day 2		Verilog HDL-2	Xilinx Vivado	NIELIT Calicut
Day 3		Synthesis and FPGA Architecture	Xilinx Vivado	NIELIT Calicut
Day 4		FPGA Design Flow- Basics	Xilinx Vivado	NIELIT Calicut
Day 5		FPGA Design Flow- Advanced IP Cores, Chipscope(ILA), VIO etc.	Xilinx Vivado	NIELIT Calicut
Day 6		Soc Design flow in Xilinx Vivado.	Xilinx Vivado	NIT Meghalaya
Day 7		Usage of FPGA Board resources at the system level.	Xilinx Vivado	NIT Meghalaya
Day 8		Integration of Verilog FIR filter to the ARM processor.	Xilinx Vivado	NIT Meghalaya
Day 9		Integration of HLS Matrix Multiplier.	Xilinx Vivado	NIT Meghalaya
Day 10		Integration of Soble edge detection in Image processing applications using DMA.	Xilinx Vivado	NIT Meghalaya

<u>Certificate</u>: e-Certificate will be mailed to the registered email address after completion of the course.

Course Materials

Lectures Notes will be made available in the LMS

<u>**Coordinators**</u>

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