National Institute of Electronics and Information Technology, Chennai

COURSE PROSPECTUS

Name of the Group:	ES Group
Name of the Course:	**Online Internship/Certificate Course** on FPGA Programming using Verilog HDL
Course Code:	VL100
Starting Date:	16th December 2021
Duration:	20 Hrs
Course Coordinator:	Ishant Kumar Bajpai, M: +91-9958016673, Email: ishant@nielit.gov.in
Last date of Registration:	13th December 2021

Preamble:

VLSI Design has become more and more common as a core technology used to build electronic systems. By integrating soft-core or hard-core processors, these devices have become complete systems on a chip, steadily displacing general purpose processors and ASICs. In particular, high performance systems are now almost always implemented with FPGAs.

As per the recently published data, there are over 20,000 engineering professionals are working in more than 150 companies in chip designing industry and there is a huge demand for high quality trained manpower in this field.

This program will enhance the career opportunities of the participants by up skilling/reskilling in Verilog hardware description language (HDL) and its use in programmable logic design. The emphasis is on the synthesis constructs of Verilog HDL; however, it will enable the participant to use FPGA architecture for a given application along with practical design skills state of the art software tools for FPGA development, and solve critical digital design problems implemented in FPGAs to achieve industry level design skills.

Objective of the Course:

Program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL and implement them in FPGA. In this process participant will acquire expertise on entire logic design process and will be able to take on the challenges posed by chip design industry.

Outcome of the Course:

After successful completion of this Course, the participants shall able to:

1. Design Control and Data path Units
2. Author Design IPs for VLSI using Verilog HDL
3. Develop Test Benches using Verilog HDL
4. FPGA based prototyping using Verilog HDL

Course Structure:

S.No	Topics	Duration (in Hrs.) Via Online Mode
1	Module 1: Hardware Description Language (Verilog HDL) • Introduction to Verilog HDL & Hierarchical Modelling Concepts • Lexical Conventions & Data Types • System Tasks & Compiler Directives • Modules, Ports and Module Instantiation Methods • Modelling methods. • Design Verification using Test benches	12
2	FPGA Architecture and Prototyping • Introduction to Programmable Logic and FPGAs • Popular CPLD & FPGA Families • Architecture of popular Xilinx and Altera FPGAs • FPGA Design Flow • Implementation Details • Advanced FPGA Design tips • Logic Synthesis for FPGA • Design problems (Mini Project)	8
Total		**20**

Other Details:

Course Fees: (Non-Refundable) **Rs.700/- (Including GST)**

However, the above registration fee shall be refunded on few special cases as given below:

1. If course postponed and new date is not convenient for the student.

2. If course cancelled.

Payment schedule: The Fee is to be paid in one instalment as given below:

Instalment No.	Last Date for Payment	Amount (in Rs.)
1.	13th December 2021	700/-

Prerequisite/Eligibility: Understanding of Basic Mathematics and enthusiasm to learn programming

How to apply:

Candidates can apply online in our website http://reg.nielitchennai.edu.in/. Payment towards non-refundable Registration and Course fee can be paid through any one of the following modes:

- Online transaction: **Beneficiary Name: NIELIT CHENNAI, Account No: 31185720641, Branch: Kottur (Chennai), IFSC Code: SBIN0001669.**
- Pay through Unified Payment Interface (UPI) payment methods eg: Google Pay, Paytm, BHIM, Phone Pe
- DD drawn from a nationalized bank (preferably SBI) in favour of ―NIELIT Chennai‖ payable at Chennai.
  Note: The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account.

Last date of Registration: 13th December 2021

Selection of candidates: Selection is based on the first come basis (subject to fulfilling the eligibility criteria)

Admission Procedure:

All interested candidates are required to fill the Registration form with the Course fees before **13th December 2021** with all the necessary following documents.

- One passport size photograph
- Self-attested copy of Govt. issued photo ID card
- Candidates may also submit the certificate of their highest qualification

All the above necessary documents have to be uploaded in the registration portal while applying for the course. Improper documents submission of candidates may lead to cancellation of admission for the course.
Note: Working days are from Monday to Friday.

Discontinuing the course: No fees under any circumstances shall be refunded in case of a student discontinuing the course. No certificate shall be issued if discontinued.

Course Timings: **3:30 PM to 5:30 PM** (2 hour online daily from Monday to Friday)

Mode of Training: Online

Certification:

For Internship Students: Certificate will be issued to all candidates who complete the course successfully

For Certificate Course students:

Certificate will be issued to the participants of based on the marks scored in the examination conducted after the completion of training. The grading pattern will be as below:

Grade	**S**	**A**	**B**	**C**	**D**	**Participation Certificate only**
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

Course enquiries: Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday

E-mail: Ishant@nielit.gov.in
Contact Person: **Ishant Kumar Bajpai, Mobile: 9958016673**

Lab Facilities: Xlinx Design tool, Atlys Spartan-6 FPGA Development Kit, DE0 Nano & DE2-115 Development Board, Xilinx Kintex-7 FPGA KC705 Evaluation Kit, Xilinx Zyng-7000 SoC Video and imaging kit, ZedBoard Zyng-7000 Development Board, and Logic Analyzer.

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Annexure

Detailed Syllabus of the Course

1. Hardware Description Language (Verilog HDL)

Duration: 12 Hours

Objective The objective of the module is to provide a thorough understanding about and hands-on with digital design & Test bench based verification using Verilog HDL.

- ✓ Introduction to Verilog HDL & Hierarchical Modelling Concepts
- ✓ Lexical Conventions & Data Types
- ✓ System Tasks & Compiler Directives
- ✓ Modules, Ports and Module Instantiation Methods
- ✓ Modelling methods.
- ✓ Design Verification using Test benches

Reading List:

1. Verilog HDL - A guide to Digital Design and Synthesis by Samir Palnitkar.
2. A Verilog HDL Primer by J.Bhasker.
3. Verilog HDL Synthesis, A Practical Primer by J. Bhasker
4. Verilog Digital System Design by Zainalabedin Navabi

2. FPGA Architecture and Prototyping

Duration: 8 Hours

Objective The objective of the module is to provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation.

- ✓ Introduction to Programmable Logic and FPGAs
- ✓ Popular CPLD & FPGA Families
- ✓ Architecture of popular Xilinx and Altera FPGAs
- ✓ FPGA Design Flow
- ✓ Implementation Details
- ✓ Advanced FPGA Design tips
- ✓ Logic Synthesis for FPGA
- ✓ Design problems (Mini Project)

Reading List:

1. FPGA Users Guides and Datasheets from Xilinx & Altera
2. FPGA-Based System Design by Wayne Wolf
3. Advanced FPGA Design Architecture, Implementation and optimization by Kilts
4. Embedded Core Design with FPGAs. by Zainalabedin Navabi
5. FPGA Prototyping by Verilog Examples by Pong P. Chu

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