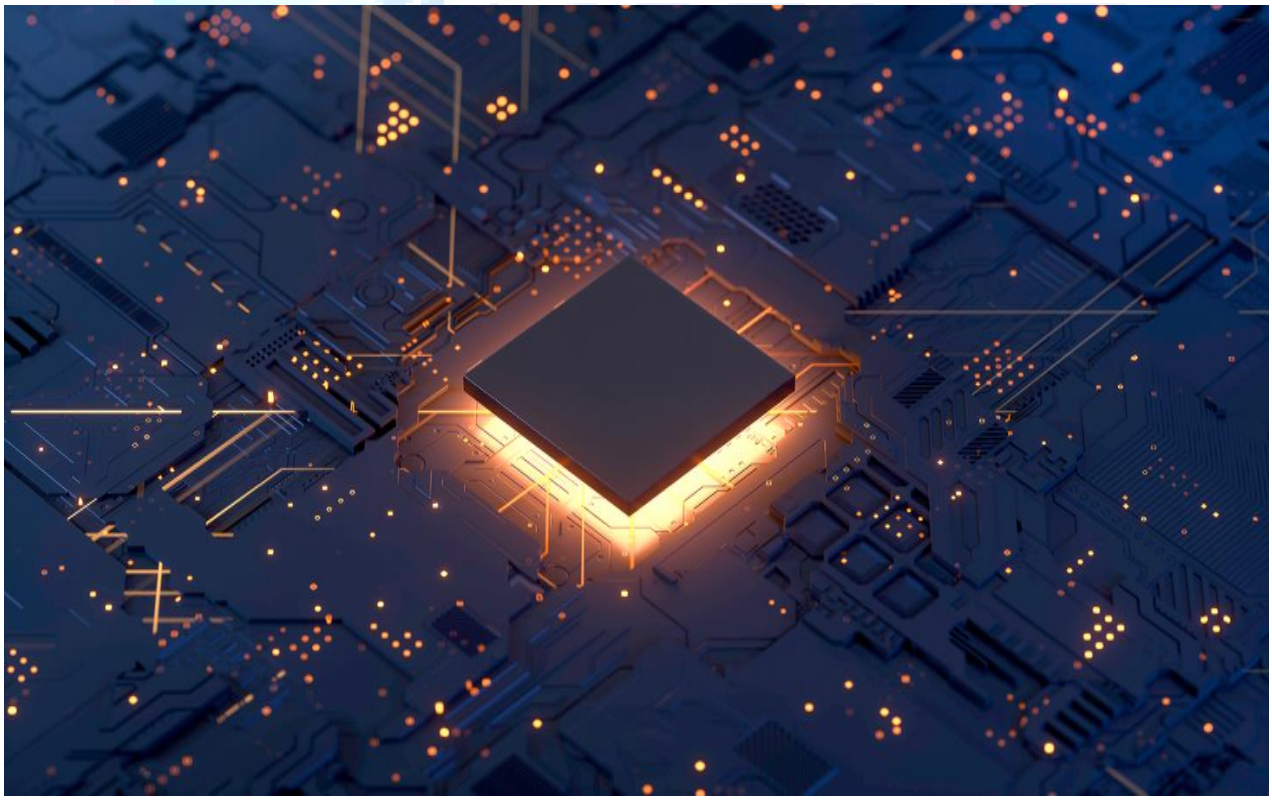
नेशनल इंस्टीट्यूट ऑफ इलेक्ट्रॉनिक्स एंड इंफॉर्मेशन टेक्नोलॉजी, चेन्नई
National Institute of Electronics and Information Technology, Chennai
Autonomous Scientific Society of Ministry of Electronics & Information Technology (MeitY), Govt. of India
ISTE Complex, 25, Gandhi Mandapam Road, Chennai - 600025

Course Prospectus

Certificate course on SoC Design for ML Applications

Mode: Online



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Course Prospectus

Course Name: Certificate course on SoC Design for ML Application

Course Code: ES 400

Duration: 420 hours

Last Date of Registration: 30-10-2022

Date of publishing Provisional Selection List: 31-10-2022

Course Start Date: 01-11-2022

Fee Details:

Registration Fee- Rs. 1,000 /- (Adjusted with Total Fee)

Total Fee – Rs. 9800 /-

Preamble:

Today SoC is prevalent in all kinds of electronics systems. From embedded systems to cloud computers, SoCs are being used in various configurations for versatile types of tasks. The growing class of complex applications such as machine learning and image processing makes it difficult for engineers to close the increasingly severe productivity gap that arises from the integration of hardware and software. The complexity challenge can only be tackled by well-trained engineers with good understanding of the requirements and challenges at all levels of the design process. Hence, there need an advanced training program that promote the integration of hardware and software as a single discipline. This course focuses on the architecture of embedded processors and its implementation on the target FPGA platform.

Objective of the Course:

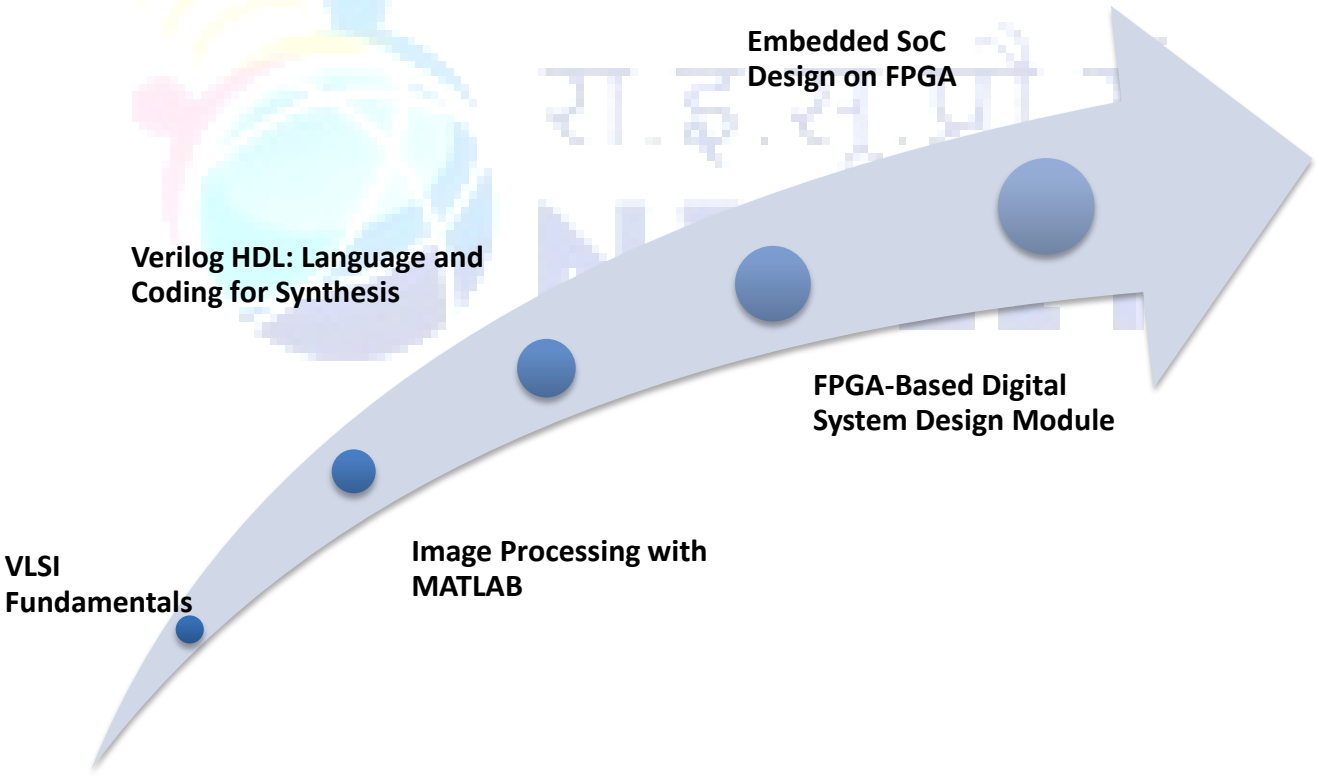
Program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL and implement them in FPGA. The qualifiers will acquire hands-on experience in state-of-the-art design methodologies and platforms.

Outcome of the Course:

After successful completion of this Course, students will be able to:

- Implement the Image Processing algorithms using MATLAB
- Design and Develop IPs for VLSI using Verilog HDL and prototype them on FPGAs
- Create their own IP and SoC design for FPGA implementation
- Develop their own software application with Zynq APSoC

Full Flow of Course



Course Structure

This course contains a total of 6 module Candidate need to qualify the each module to qualify the Certificate course on SoC Design for ML Application.

Module Code	Module Name	Duration(in Hours)
ES 401	VLSI Fundamentals	70
ES 402	Image Processing with MATLAB	70
ES 403	Verilog HDL: Language and Coding for Synthesis	70
ES 404	FPGA-Based Digital System Design Module	70
ES 405	Embedded SoC Design on FPGA	70
ES 406	Project	70
	Total Duration	**420**

Course Fees

The course fee is Rs. 9800/- Including GST.

**GST is Applicable as per Govt. Norms GST (currently it is 18%).*

Registration Fee.

(**Non-Refundable if candidate is selected for admission but did not join and if a candidate has applied but not eligible.)**

Rs. 1,000/- (Adjustable with Total fee for candidates).

However, the above registration fee shall be refunded on few special cases as given below

- ✓ Candidates are eligible but not selected for admission.
- ✓ Course postponed and new date is not convenient for the student.
- ✓ Course cancelled.

Eligibility

- ✓ Final Year Polytechnic Diploma in Electronics/Electrical/ Instrumentation

or

- ✓ 5th semester B.E/B.Tech in Computer Science, IT, Electronics/Electronics & Communication/ Electrical/ Electrical & Electronics/Instrumentation, biomedical or aligned branches

Number of Seats: 30 – Total

Category	No. of Seats
SC (15%)	4
ST (7.5%)	2
GENERAL	24
Total	**30**

Note: Seats are allocated based on the merit of the Qualification.

How to Apply?

Candidates can apply online in our website http://reg.nielitchennai.edu.in. Payment towards non-refundable registration fee can be paid through any of the following modes:

- ✓ Online transaction: Account Name: NIELIT CHENNAI, Account No: 31185720641, Bank name: State Bank of India (SBI), Branch: Kottur (Chennai), IFSC Code: SBIN0001669.
- ✓ Pay through UPI Mobile Apps

Note: *The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

Last date of Registration: 30-10-2022

Registration Procedure

All interested candidates are required to fill the Registration form online with registration fees before 30th October 2022 with all the necessary information.

Selection Criteria of candidates

The selection to the course shall be based on the following criteria:

Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

- ✓ The first list of Provisionally Selected Candidates will be published on NIELIT Chennai website (www.nielit.gov.in/chennai) 31st October 2022 by **5:00 PM**. In case of vacancy, an additional selection list will be prepared and the selection will be intimated by email only.
- ✓ Provisionally selected candidate has to upload their document on registration portal for online verification.

  - Original Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheets & Degree Certificate/Course Completion Certificate based on the eligibility criteria), 10th and 12th mark sheet.
  - One passport size photograph.
  - Self-attested copy of Govt. issued photo ID card

- ✓ After document verification, selected candidates have to pay **Rs. 8,800** /- on or before **01-11-2022** by payment mode mentioned above. Selected candidates are requested to upload the proof of remittance of fee on registration portal and also send the proof of remittance of fee as email to ishant[at]nielit[dot]gov[dot]in / trng[dot]chennai[at]nielit[dot]gov[dot]in.

Admission:

All provisionally selected candidates whose documents are verified and paid the fees (full or first instalment) and verified by accounts section of NIELIT Chennai will get a welcome message in his/her login ID provided during registration. The Credential and URL for online portal will be shared through WhatsApp or email.

Discontinuing the course

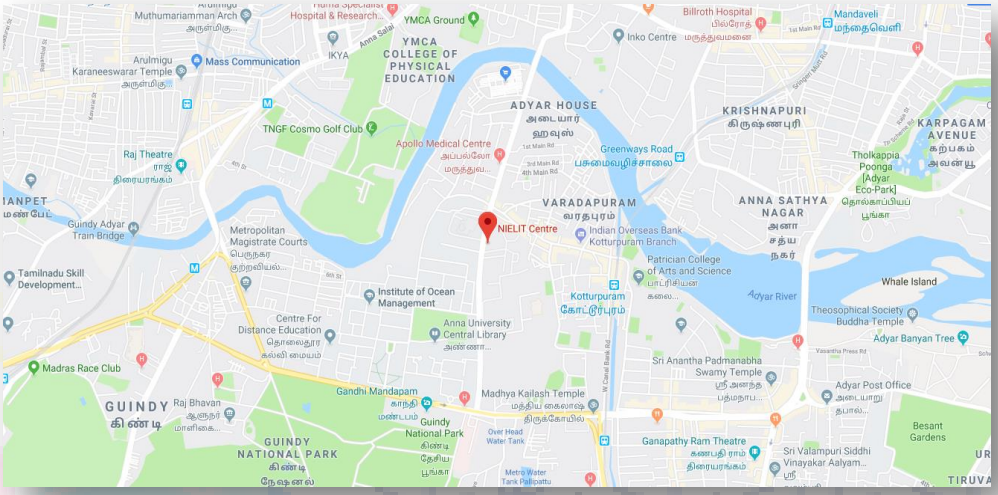
- ✓ No fees (including the security deposit) under any circumstances, shall be refunded in the event of a student who have completed the process of admission or discontinuing the course in between. No certificate shall be issued for the classes attended. Only Grade Sheet will be issued.
- ✓ If candidates are not uploading consecutive 3 assignments within assigned time their candidature will be cancelled without any notice and all fees paid will be forfeited.
- ✓ If candidates are not appearing for any internal examinations/practical their candidature will be cancelled without any notice and all fees paid will be forfeited

Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The cloud based online theory classes will be on forenoon and lab session will be conducted mostly on afternoon time.

Location:

NIELIT Chennai is located at Gandhi Mandapam Road, Kotturpuram, Chennai (Landmark: Opp.To Anna Centenary Library).



Address:

National institute of Electronics and Information Technology

ISTE Complex, No. 25, Gandhi Mandapam Road, Chennai – 600025

E-mail: ishant[at]nielit[dot]gov[dot]in/ Phone: 044-24421445

Contact Person: Mr. Ishant Kumar Bajpai Mobile: 99580 16673 (Call @ 9 AM to 6 PM)

Course enquiries

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

Placement:

Students, who have completed the course successfully and qualified, will be provided placement assistance on core companies.

Important Dates

Last Date of Registration: 30-10-2022

Date of publishing Provisional Selection List: 31-10-2022

Course Start Date: 01-11-2022

Last Date to make full payment: 01-11-2022

Examination & Certification

- ✓ Final Certificates will be issued after successful completion of all the modules. For getting certificate a candidate has to pass each module individually with minimum required marks of 50%.

Examination Scheme

Examination scheme for each module is as follows:

Module Name	Total Marks	Written	Practical / Assignment
VLSI Fundamentals	**100**	25	75
Image Processing with MATLAB	**100**	25	75
Verilog HDL: Language and Coding for Synthesis	**100**	20	80
FPGA-Based Digital System Design Module	**100**	25	75
Embedded SoC Design on FPGA	**100**	25	75
Project	**100**	0	100
Total	**600**	**120**	480

Grading Scheme

- ✓ Following Grading Scheme (on the basis of total marks) will be followed:

Grade	S	A	B	C	D	Fail
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

- ✓ Final Grading as per above grading scheme will be given on the basis of total marks obtained in all modules.
- ✓ Candidate not eligible for grade certificate will be awarded a participation certificate.

Lab Infrastructure Details:

Hardware Facilities:

- ✓ FPGA-Zed Board,
- ✓ Kintex, Virtex, Zynq,
- ✓ DE0 Development,
- ✓ Anvyl & Atlys Spartan-6,
- ✓ Zybo Board

Software Facilities:

- ✓ OpenSTM, CubeMX
- ✓ Xilinx Vivado
- ✓ Xilinx Vitis
- ✓ Matlab

Director, NIELIT Chennai

Dr. Pratap Kumar S

Director

Dr. Pratap Kumar S, is B.Tech (Electrical Engineering), M.Tech (Digital Electronics), MBA (Marketing) and PhD (Strategic Management). He has More than 29 years' experience in planning and execution of industrial consultancy projects, and capacity building projects funded by both industry and central & state ministries. Executed 7 major industrial consultancy projects and associated with the development of more than 50 product technologies, empowered more than 10,000 candidates through various capacity building programs and facilitated more than 40,000 job seekers through various job fairs and outreach programs. He has expertise in Strategy, Product Development, Automotive Electronics, Embedded Systems, and Power Electronics.

Faculty Profile:

Ishant Kumar Bajpai

Scientist 'C'

Ishant Kumar Bajpai, Scientist 'C', NIELIT Chennai Has more than 8 years' experience in Coordination and Implementation of funded projects in the area of IoT and VLSI with the application in Biomedical & Automotive. He has successfully executed 1 funded capacity building project in Karnataka & Kerala State and involved in the implementation of 4 skill development /capacity building projects funded by MeitY in the states of Tamil Nadu, Andhra Pradesh and Telangana. Before joining the NIELIT, he was working as a Scientific Officer in the IT Research Academy Division of Digital India Corporation (erst. Media Lab Asia), where he was involved in the Project Planning, Design and Implementation of projects in the domain of Mobile Computing, Networking & Applications.

Balakumar V

Resource Person-PA

Balakumar , Resource Person-PA having 2 years of experience in handing training sessions and Labs on Electronic systems, Image Processing with the background of Deep Learning and its implementation on FPGA .

ANUMOL C S

Resource Person- (Embedded & VLSI)

Anumol C S, Resource Person- Embedded and VLSI having knowledge in VLSI domain with the background of MTech in Electronics and Communication Engineering.

Annexure

Detailed Syllabus of the Course

ES401: VLSI Fundamentals

Objective:

The objective of the module is to provide a detailed review of VLSI fundamentals for a thorough understanding of the concepts and techniques for analog and digital system design.

Outcomes:

On successful completion of the module, the candidate shall be able to:

- Design and analyse analog as well as digital systems

Duration: 70 Hours

Course Description

Analog Concepts

- Introduction to VLSI
- MOS Circuit Model, Biasing of Circuits
- Amplifiers, MOS Amplifiers
- Frequency Response of Amplifier
- Differential Amplifier
- Feedback Theory
- OPAMP Circuits

Digital Concept

- Combinational Circuit Design
- Sequential Circuit Design including clocking and reset concepts
- Design of controller and Data path units
- State Machines
- Design Examples & Case Studies

ES 402: Image Processing with MATLAB

Objective

The objective of the module is to provide a thorough understanding of and hands-on with geometric Transformation of Imaging using MATLAB

Outcomes

After successful completion of the module, the students shall be able to:

- Understand the geometric Transformation of Image
- Implement the Image Processing application using MATLAB

Duration: 70 Hours

Course Description

- Introduction to Image Processing
- Notion of pixel, resolution, quantization, photon noise, Geometric transformations,
- source-to-target and target-to-source mapping, planar and rotational homography,
- Image registration and change detection,
- Motion Blur and Image Formation
- Image Transform
- Image Enhancement, Restoration, and Edge Detection Design Verification using Test benches
- Typical image processing application implementation using MATLAB

ES 403: Verilog HDL: Language and Coding for Synthesis

Objective

The objective of the module is to provide a thorough understanding of and hands-on with digital design & Verification using Verilog HDL

Outcomes

After successful completion of the module, the students shall be able to:

- Design IPs for VLSI using Verilog HDL
- Develop Test benches using Verilog HDL

Duration: 70 Hours

Course Description

- Introduction to Verilog HDL & Hierarchical Modelling Concepts
- Lexical Conventions & Data Types
- System Tasks & Compiler Directives
- Modules, Ports, and Module Instantiation Methods
- Gate Level Modelling
- Dataflow Modelling
- Behavioural Modelling
- RTL Design and Logic Synthesis and Synthesis issues
- Design Verification using Test benches
- Mini-project and Case Studies

ES 404: FPGA Based Digital System Design Module

Objective

The objective of the module is to provide a thorough understanding about and hands-on practice with FPGA based digital system design and emulation

Outcomes

After successful completion of this module, students should be able to:

- Prototype digital Systems using FPGA
- Emulate, debug & Characterize reusable IPs

Duration: 70 Hours

Course Description

- Introduction to Programmable Logic and FPGAs
- Architecture of popular Xilinx FPGAs
- FPGA Design Flow Xilinx Vivado®
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Implementation Details and optimization techniques
- Static Timing Analysis
- Introduction to AXI4/Avalon Interfaces
- Design problems using Xilinx® Platforms
- Case Studies on FPGA-Based implementations

ES 405: Embedded SoC Design on FPGA

Objective

The objective of this module is to enable the participant to optimize throughput and adapt processors to meet the specific needs of different Image processing/ML architectures by the effective implementation on FPGAs.

Outcomes

After successful completion of the module, the students shall be able

- Create their own IP and SoC design for FPGA implementation
- Perform in-system Hardware-debugging of the post-implemented design
- Develop their own software application with Zynq APSoC

Duration: 70 Hours

Course Description

VLSI implementation architectures for Image Processing/ML

- Multi-core, many-core, and hardware accelerators
- Hardware acceleration of Image Processing Algorithms
- Design steps- Software Design Flow, Platform Project Creation, Application Project Creation, and Debugging using Xilinx Vitis
- Case Studies: Realization of Image Processing algorithms on FPGA
-

Metrics for Analysis and Comparison of Architectures

- Hardware performance matrices-Processing time and a maximum frequency of operation, memory footprint, etc.
- Performance comparison with DSPs and Multi-core SoCs.

ES 406: Project Work Module

Duration: 70 Hours

Description

The students can select hardware, software or system level projects. The project can be implemented using FPGAs and Hardware Platforms which students have studied and used during the course.

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