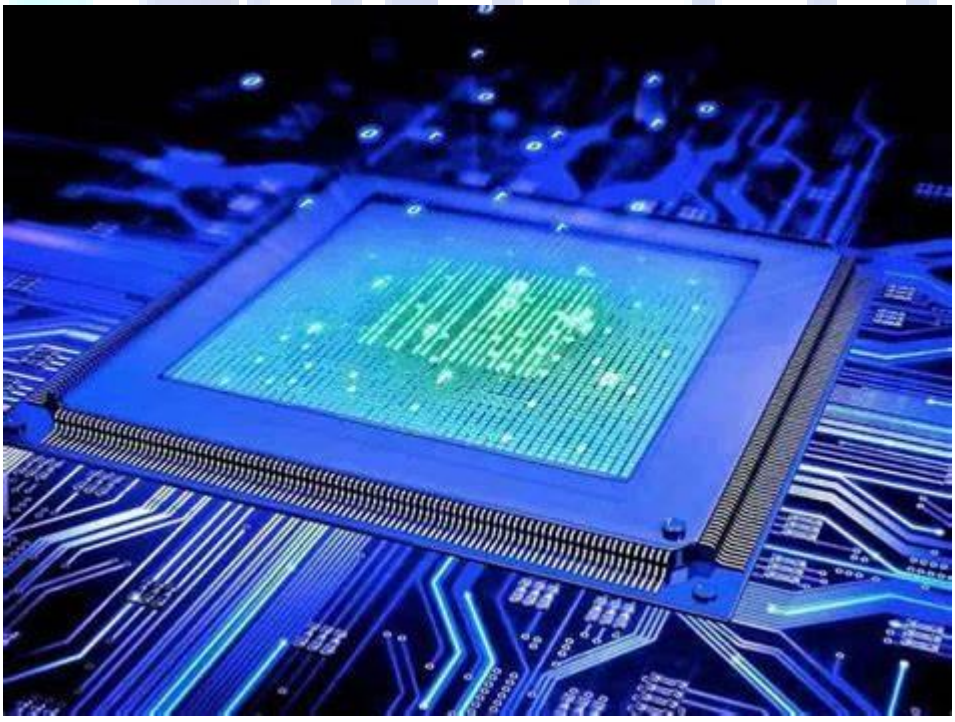
नेशनल इंस्टीट्यूट ऑफ इलेक्ट्रॉनिक्स एंड इंफॉर्मेशन टेक्नोलॉजी, चेन्नई
National Institute of Electronics and Information Technology, Chennai
Autonomous Scientific Society of Ministry of Electronics & Information Technology (MeitY), Govt. of India
ISTE Complex, 25, Gandhi Mandapam Road, Chennai - 600025

Course Prospectus

Foundation course in VLSI Design
NSQF Level 4

Mode: Online



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NIELIT

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Course Prospectus

Course Name: Foundation course in VLSI Design (Online Mode)

Course Code: ES 200

Duration: 90 Hours

Last Date of Registration: 30-10-2022

Date of publishing Provisional Selection List: 31-10-2022

Last date to make payment: 01-11-2022

Course Start Date: 01-11-2022

Fee Details:

Registration Fee- Rs. 1000/- (Adjusted with Total Fee)

Total Fee - Rs. 6300/- (NIL for SC/ST Candidates)

Preamble:

VLSI Design has become more and more common as a core technology used to build electronic systems. By integrating soft-core or hard-core processors, these devices have become complete systems on a chip, steadily displacing general-purpose processors and ASICs. In particular, high-performance systems are now almost always implemented with FPGAs.

As per the recently published data, there are over 20,000 engineering professionals working in more than 150 companies in the chip designing industry and there is a huge demand for high-quality trained manpower in this field. This program will enhance the career opportunities of the participants in upskilling/reskilling in Verilog hardware description language (HDL) and its use in programmable logic design. The emphasis is on the synthesis constructs of Verilog HDL; however, it will enable the participant to use FPGA architecture for a given application along with practical design skills state of the art software tools for FPGA development, and solve critical digital design problems implemented in FPGAs to achieve industry level design skills.

Objective of the Course:

Program aims to enable participants to design reusable Intellectual Property (IP) Cores as building blocks using Verilog HDL and implement them in FPGA. In this process, participants will acquire expertise on entire logic design process and will be able to take on the challenges posed by chip design industry.

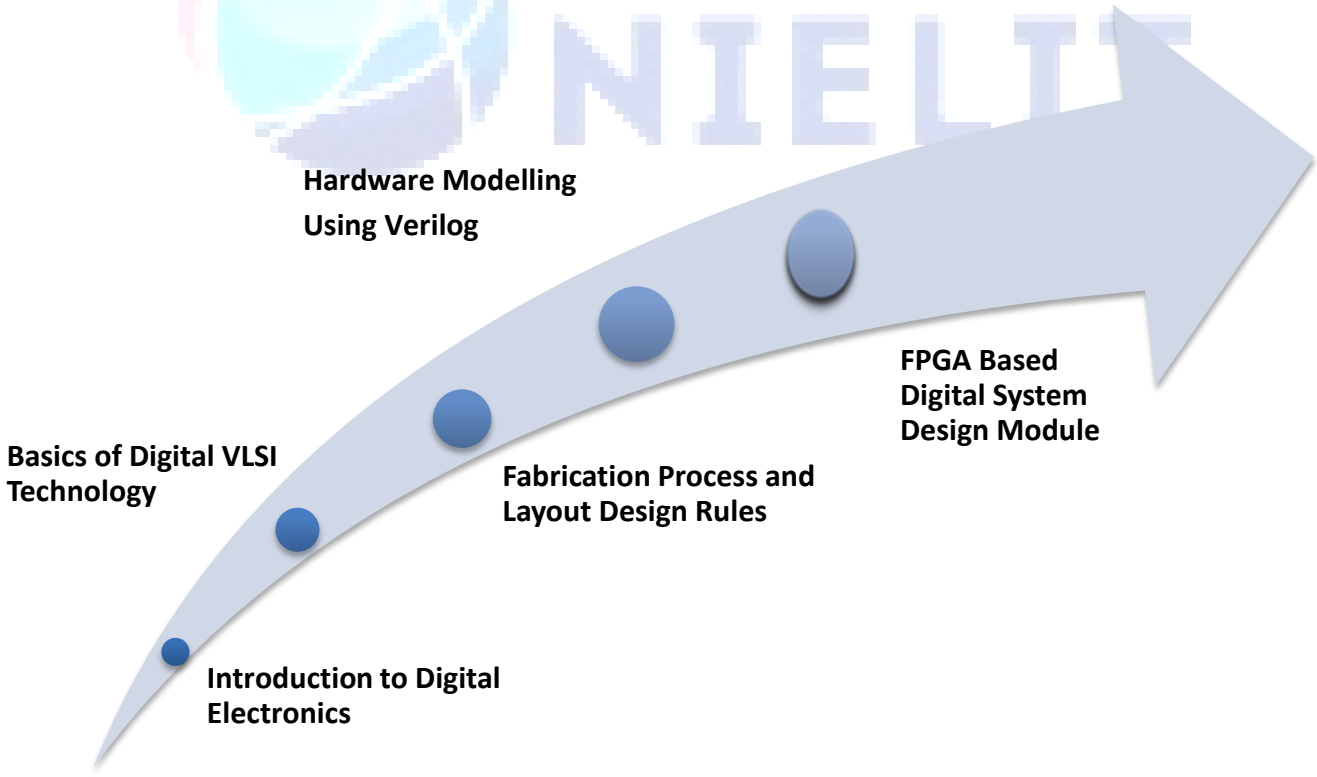
Outcome of the Course:

After successful c

ompletion of this Course, students will be able to:

- Understand brief history, present and future and Design Cycle of VLSI technology. Understand the Design Cycle of VLSI.
- Understand Verilog programming syntax. Level of Abstraction in Verilog programing writing and simulating test benches in Verilog.
- Design and Develop IPs for VLSI using Verilog HDL and prototype them on FPGAs
- Emulate, debug & Characterize reusable IPs

Full Flow of Course



Course Structure

This course contains a total of 6 module Candidate need to qualify the each module to qualify the Foundation course in VLSI Design program.

Module Code	Module Name	Duration(in Hours)
ES 201	Introduction to Digital Electronics	10
ES 202	Basics of Digital VLSI Technology	10
ES 203	Fabrication Process and Layout Design Rules	10
ES 204	Digital CMOS Design	10
ES 205	Hardware Modelling Using Verilog	20
ES 206	FPGA Based Digital System Design Module	30
	Total Duration	**90**

Course Fees

Course fee is Rs. 6300/- Including GST.

Registration Fee	Rs. 1000/- for SC-ST (Refundable *)	Rs. 1000/- for others (Adjustable with total fee)	
	SC-ST Candidates (Fee including GST in Rs.)	General Candidates (Fee including GST in Rs.)	Last Date
Total	NIL	6300	01-11-2022
***Caution deposit (Rs. 1000/-) will be refunded for eligible SC/ST candidates who will be successfully completing the course with NSQF certification under SCSP/TSP scheme.**			

**GST is Applicable as per Govt. Norms GST (currently it is 18%).*

Registration Fee.

(**Non-Refundable if candidate is selected for admission but did not join and if a candidate has applied but not eligible.)**

However, the above registration fee shall be refunded on few special cases as given below

- ✓ Candidates are eligible but not selected for admission.
- ✓ Course postponed and new date is not convenient for the student.
- ✓ Course cancelled.

Eligibility

Final Year Polytechnic Diploma in Electronics/Electrical/ Instrumentation

or

3rd semester B.E/B.Tech in Electronics/Electronics & Communication/ Electrical/ Electrical & Electronics/Instrumentation

Number of Seats: 30 – Total

Category	No. of Seats
SC (15%)	4
ST (7.5%)	2
GENERAL	24
Total	**30**

Note: Seats are allocated based on the merit of the Qualification.

How to Apply?

Candidates can apply online in our website http://reg.nielitchennai.edu.in. Payment towards non-refundable registration fee can be paid through any of the following modes:

- ✓ Online transaction: Account Name: NIELIT CHENNAI, Account No: 31185720641, Bank name: State Bank of India (SBI), Branch: Kottur (Chennai), IFSC Code: SBIN0001669.
- ✓ Pay through UPI Mobile Apps

Note: *The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account*

Last date of Registration: 30-10-2022

Registration Procedure

All interested candidates are required to fill the Registration form online with registration fees before **30th October, 2022** with all the necessary information.

Selection Criteria of candidates

The selection to the course shall be based on the following criteria:

Selection of candidates will be based on their marks in the qualifying examination subject to eligibility and availability of seats.

- ✓ The first list of Provisionally Selected Candidates will be published on NIELIT Chennai website (www.nielit.gov.in/chennai) **31th October, 2022** by **5:00 PM**. In case of vacancy, an additional selection list will be prepared and the selection will be intimated by email only.
- ✓ Provisionally selected candidate has to upload their document on registration portal for online verification.

- ✓ **For SC/ST :**
  - Original Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheet & Degree Certificate/Course Completion Certificate), 10th and 12th mark sheets.
  - Self-attested copy of community certificate.
  - One passport size photograph.

- ✓ **For Others (General, OBC, EWS) :**
  - Original Copies of Proof of Age, Qualifying Degree (Consolidated Mark sheet & Degree Certificate/Course Completion Certificate), 10th and 12th mark sheet.
  - One passport size photograph.
  - Self-attested copy of Govt. issued photo ID card

- ✓ After document verification, selected candidates (other than SC-ST) have to pay **Rs.5300/-** or as applicable on or before **01-11-2022** by payment mode mentioned above. Selected candidates are requested to upload the proof of remittance of fee on registration portal and also send the proof of remittance of fee as email to ishant[at]nielit[dot]gov[dot]in / trng[dot]chennai[at]nielit[dot]gov[dot]in.

Admission:

All provisionally selected candidates whose documents are verified and paid the fees and verified by accounts section of NIELIT Chennai will get a welcome message in his/her login ID provided during registration. The Credential and URL for online portal will be shared through WhatsApp or email.

Discontinuing the course

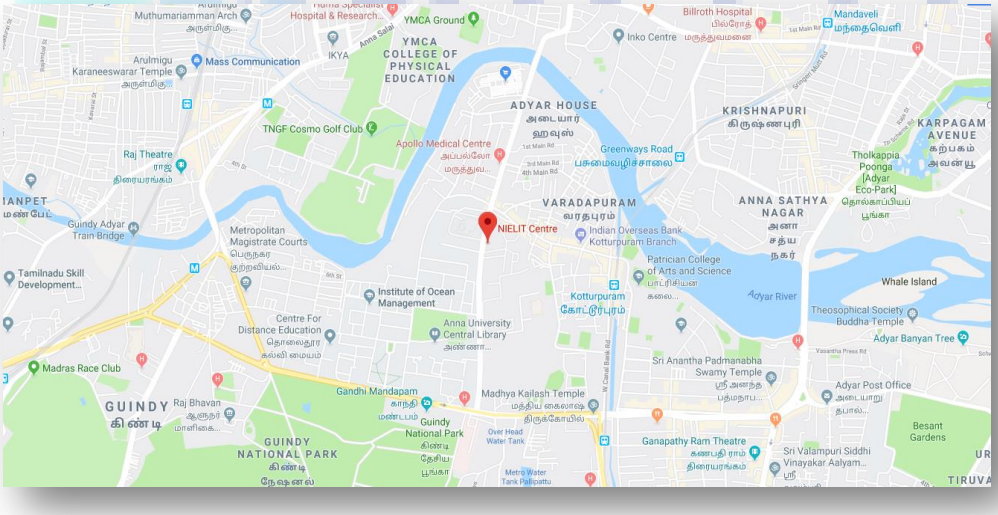
- ✓ No fees (including the security deposit) under any circumstances, shall be refunded in the event of a student who have completed the process of admission or discontinuing the course in between. No certificate shall be issued for the classes attended. Only Grade Sheet will be issued.
- ✓ If candidates are not uploading consecutive 3 assignments within assigned time their candidature will be cancelled without any notice and all fees paid will be forfeited.
- ✓ If candidates are not appearing for any internal examinations/practical their candidature will be cancelled without any notice and all fees paid will be forfeited

Course Timings:

This program is a practical oriented one and hence there shall be more lab than theory classes. The cloud based online theory classes will be on forenoon and lab session will be conducted mostly on afternoon time.

Location:

NIELIT Chennai is located at Gandhi Mandapam Road, Kotturpuram, Chennai (Landmark: Opp.To Anna Centenary Library).



Address:

National institute of Electronics and Information Technology
ISTE Complex, No. 25, Gandhi Mandapam Road, Chennai – 600025
E-mail: ishant[at]nielit[dot]gov[dot]in/ Phone: 044-24421445

Contact Person: Mr. Ishant Kumar Bajpai Mobile: 99580 16673 (Call @ 9 AM to 6 PM)

Course enquiries

Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

Placement:

Students, who have completed the course successfully and qualified, will be given placement guidance and career counselling to crack the interviews.

Important Dates

Last Date of Registration: 30-10-2022

Date of publishing Provisional Selection List: 31-10-2022

Last Date of making the payment: 01-11-2022

Course Start Date: 01-11-2022

Examination & Certification

- ✓ Final Certificates will be issued after successful completion of all the modules. For getting certificate a candidate has to pass each module individually with minimum required marks of 50%.

Examination Scheme

Internal examination scheme for each module is as follows:

Module Name	Total Marks	Written	Practical / Assignment
Introduction to Digital Electronic	**50**	10	40
Basics of Digital VLSI Technology	**50**	10	40
Fabrication Process and Layout Design Rules	**50**	10	40
Digital CMOS Design	**50**	10	40
Hardware Modelling Using Verilog	**75**	20	55
FPGA Based Digital System Design Module	**125**	25	100
Total	**400**	**85**	**315**

Grading Scheme

✓ Following Grading Scheme (on the basis of total marks) will be followed:

Grade	S	A	B	C	D	Fail
Marks Range (in %)	85 to 100	75 to 84	65 to 74	55 to 64	50 to 54	Below 50

✓ Final Grading as per above grading scheme will be given on the basis of total marks obtained in all modules.

✓ NSQF Examination Pattern:

Theory (Each Question will carry 1 mark) Duration (in Min): 90		Practical Duration (in Min): 180		Internal Assessment (Marks)	Project/ Presentation/ Assignment (Marks)	Total
Papers	Marks / Paper	Papers	Marks/ Paper			
1	100	1	60	20	20	200

Lab Infrastructure Details:

Hardware Facilities:

- ✓ FPGA-Zed Board,
- ✓ Kintex, Virtex, Zynq,
- ✓ DE0 Development,
- ✓ Anvyl & Atlys Spartan-6,
- ✓ Zybo Board

Software Facilities:

- ✓ Xilinx Vivado
- ✓ Xilinx Vitis
- ✓ Matlab

Director, NIELIT Chennai

Dr. Pratap Kumar S

Director

Dr. Pratap Kumar S, is B.Tech (Electrical Engineering), M.Tech (Digital Electronics), MBA (Marketing) and PhD (Strategic Management). He has More than 29 years' experience in planning and execution of industrial consultancy projects, and capacity building projects funded by both industry and central & state ministries. Executed 7 major industrial consultancy projects and associated with the development of more than 50 product technologies, empowered more than 10,000 candidates through various capacity building programs and facilitated more than 40,000 job seekers through various job fairs and outreach programs. He has expertise in Strategy, Product Development, Automotive Electronics, Embedded Systems, and Power Electronics.

Faculty Profile:

Ishant Kumar Bajpai

Scientist 'C'

Ishant Kumar Bajpai, Scientist 'C', NIELIT Chennai Has more than 8 years' experience in Coordination and Implementation of funded projects in the area of IoT and VLSI with the application in Biomedical & Automotive. He has successfully executed 1 funded capacity building project in Karnataka & Kerala State and involved in the implementation of 4 skill development /capacity building projects funded by MeitY in the states of Tamil Nadu, Andhra Pradesh and Telangana. Before joining the NIELIT, he was working as a Scientific Officer in the IT Research Academy Division of Digital India Corporation (erst. Media Lab Asia), where he was involved in the Project Planning, Design and Implementation of projects in the domain of Mobile Computing, Networking & Applications.

Balakumar V

Resource Person-PA

Balakumar , Resource Person-PA having 2 years of experience in handing training sessions and Labs on Electronic systems, Image Processing with the background of Deep Learning and its implementation on FPGA .

ANUMOL C S

Resource Person- (Embedded & VLSI)

Anumol C S, Resource Person- Embedded and VLSI having knowledge in VLSI domain with the background of MTech in Electronics and Communication Engineering.

Annexure

Detailed Syllabus of the Course

ES 201: Introduction to Digital Electronics

Duration: **10** Hours

Course Description

- Number System
- Logic Gates
- Latches and Flip Flops
- Combinational Logic Circuit
- Sequential Logic Circuit

ES 202: Basics of Digital VLSI Technology

Duration: **12** Hours

Course Description

- Historical Perspective.
- VLSI technology trends performance measures and Moore's law comparisons of technology trends.
- Introduction to the family of Transistor.
- Basics of CMOS Transistor
- MOSFET Fabrication Process
- INVERTERS
- VLSI Design Flow
- Introduction to ASIC & FPGA

ES 203: Fabrication Process and Layout Design Rules

Duration: **6** Hours

Course Description

- Fabrication Process and Layout Design Rules
- Introduction to fabrication Process.
- General Aspects of CMOS Technology.
- CMOS Inverter Fabrication Process.
- Layout Design Rules.
- Semi-Custom Design Flow
- Full-Custom Design Flow

ES204: Digital CMOS Design

Duration: **12** Hours

Course Description

- CMOS Inverter Basics.
- Inverter Transfer Characteristics.
- Inverter sizing.
- Inverter Design.
- Other types of Inverter and its problem.

ES205: Hardware Modelling Using Verilog

Duration: **28** Hours

Course Description

- Introduction to Verilog
- Programming Structure
- Level of Abstraction
- Data Type
- Behavioural Modelling and Timing
- Verilog PROCEDURAL ASSIGNMENT
- Introduction to BLOCKING NON-BLOCKING ASSIGNMENTS in Verilog
- Verilog Functions
- Verilog User Defined Primitives
- Writing Very First Program
- WRITING TEST BENCHES in Verilog
- Verilog Simulation Basics

ES 206: FPGA Based Digital System Design Module

Duration: 30 Hours

Course Description

- Introduction to Programmable Logic and FPGAs
- Architecture of popular Xilinx FPGAs
- FPGA Design Flow Xilinx Vivado®
- Advanced FPGA Design tips
- Logic Synthesis for FPGA
- Implementation Details and optimization techniques
- Static Timing Analysis
- Introduction to AXI4/Avalon Interfaces
- Design problems using Xilinx® Platforms
- Case Studies on FPGA-Based implementations

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