National Institute of Electronics &Information Technology Aurangabad
CEDTI Complex, Dr. B.A.M. University campus
Aurangabad, Maharashtra-431004
http://www.nielit.gov.in/aurangabad/

Ministry of Electronics and Information Technology
Government of India

Online Certificate Course in VLSI Design

Course Duration- 2 Weeks **Timings-(10:00am to 1:00pm)**
Theory-1Hr & Lab-1 Hrs. **Total- 2 Hrs. per Day**
Start Date-12thMay 2021

Course Description:-

- Hardware Modelling Overview
- VHDL/Verilog language concepts
- Test benches Writing
- Coding For Synthesis
- FPGA Architecture - Basic Components of FPGA (LUT, CLB, Switch Matrix, IOB),
- FPGA Architecture of different families: 7-series and UltraScale devices, Zynq
- FPGA Design Flow - Xilinx Vivado tool Flow, Reading Reports, and Implementing IP cores
- Optimal FPGA Design - HDL Coding Techniques for FPGA, FPGA Design Techniques,
- Synthesis Techniques, Implementation Options

Eligibility:- Diploma/B.Sc/M.Sc/B.Tech/M.Tech in Electronics/Electrical/ Instrumentation/Science stream (Completed or Pursuing)

Prerequisite:- Basic Knowledge of Analog & Digital circuits.

Fee & Important dates:-

Course Fee	Rs. 2000/- incl. GST & all other charges.
Last Date for Registration & Payment	11thMay 2021
Course Start Date	12thMay 2021

Mode of Course Delivery:-The course would be conducted in a virtual classroom environment which will be completely online, Course content includes Online Theory & lab sessions, Live interactive doubt clearance sessions, Course material in text/pdf format, Links to external resources and blogs, Online Forums, Lab Assignments, Tests etc.

Certificate:-Certificate will be provided to the participants, based on minimum 80% attendance and on performance (minimum 50% marks) in the online test, conducted at the end of the course.

How to Apply:-

- Read the course structure & course requirements carefully.
- Visit the Registration portal and click on apply button.
- Create your login credentials, fill up all the required details, check preview and Submit the application form.
- Loginwith your credentialsto verify the mobile number, email ID and then uploadthe documents, Lock the profile and Pay the Fees online, using ATM-Debit Card / Credit Card / Internet Banking / UPI etc.

Course Coordinator:-

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Course Content

Day	Theory Topics	Lab Assignments
Day 1	➢ Introduction to VHDL :	➔ How to download and Install Vivado Software ➔ Install web pack License on Vivado
Day 2	➢ Introduction to Verilog	➔ How to create Project in Vivado with example
Day 3	➢ Introduction to Structural modeling ➢ Introduction to Behavioral modeling ➢ Introduction to Data Flow modeling ➢ Introduction to Mixed modeling	➔ How to write Test bench waveform with example
Day 4	➢ Introduction to ASIC and FPGA- FPGA design flow	➔ How to write constrain files in vivado
Day 5	➢ Introduction To combinational Circuits and its various examples	➔ Synthesis combinational logic Examples
Day 6	➢ Introduction To combinational Circuits and its various examples ➢ Introduction To Sequential Circuits and its various examples	➔ Synthesis sequential logic Examples
Day 7	➢ Introduction To Sequential Circuits and its various examples ➢ Introduction To FSM Circuits and its various examples	➔ Synthesis FSM Examples
Day 8	➢ Introduction To FSM Circuits and its various examples	➔ How to use IP in vivado
Day 9	➢ Practices Examples	➔ Practices Examples & Some Practicals using Basys-3 Board
Day 10	➢ Mini Project	➔ Complete Mini Project