B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

IMPORTANT INSTRUCTIONS:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2. **PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS **TOTAL MARKS: 100**

(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 64K memory contains _____ words of 8 bits each?
A) 65,536
B) 64,536
C) 65,436
D) 65,546

1.2 Which one of the following CPU registers holds the address of the instructions (instructions in the program stored in memory) to be executed next?
A) MAR (Memory address register)
B) MBR (Memory Buffer Register)
C) IR (Instruction Register)
D) PC (Program Counter)

1.3 What are the major components of a CPU?
A) Control Unit, Register Set, Arithmetic Logic Unit
B) Control Unit, Memory Unit, Arithmetic Logic Unit
C) Memory Unit, Arithmetic Logic Unit, Auxiliary Memory
D) Register Set, Control Unit, Memory Unit

1.4 What is Q, when S = 1 and R = 1 for SR flip-flop?
A) No Change
B) Indeterminate
C) Set to 1
D) Complement of previous output

1.5 To convert octal code to binary code which of the following digital functions should be used?
A) Decoder
B) Encoder
C) Multiplexer
D) Demultiplexer

1.6 A full-adder is simply a connection of two half-adders joined by
A) AND gate
B) OR gate
C) NAND gate
D) NOR gate

1.7 The CPU nearly delays its operation for one memory cycle, to allow direct memory I/O transfer. This process is called,

A) Burst transfer
B) Cycle waiting
C) Cycle stealing
D) Cycle interrupting

1.8 What are the building blocks of combinational circuits?

A) Flip-flops
B) Logic gates
C) Latches
D) Registers

1.9 The expression x + xy = x is called,

A) Commutative Law
B) Associative Law
C) Distributive Law
D) Absorption Law

1.10 Boolean functions expressed as a _____ of minterms or _____ of maxterms are said to be in a canonical form.

A) Product, Sum
B) Sum, Product
C) Subtract, Divide
D) Divide, Subtract

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 Instruction register stores address of the next instruction.

2.2 A divide-overflow condition occurs if the high-order half bits of the dividend constitute a number greater than or equal to the divisor.

2.3 A⊕B is the equation for the sum in the full adder, where A and B are input variables.

2.4 The routine executed in response to an interrupt request is called interrupt service routine.

2.5 Serial to parallel data conversion is done using counter.

2.6 Speakers can be called as a peripheral device.

2.7 D stands for Delay in D-flip flop.

2.8 A computer has memory of 256k words of 32 bits each. 16 bits are required to specify the address part.

2.9 Cache memory reduces memory access time.

2.10 MDR is not involved in memory write operation.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

X		Y	
3.1	Formula for XOR gate	**A.**	effective address
3.2	The ROM position of main memory is needed for storing _____	**B.**	memory Read
3.3	_____flip-flops make up a register of 8 bits	**C.**	3
3.4	Target address in a branch type instruction.	**D.**	432
3.5	The number of select input lines in an 8-to-1 multiplexer	**E.**	99
3.6	DR ← M [AR]	**F.**	A'B+B'A
3.7	(r-1)'s complement of 345 in octal number system	**G.**	pipeline
3.8	Decimal number equivalent to 1100011	**H.**	indirect address
3.9	Sequential circuit	**I.**	bootstrap loader
3.10	Set of data processing elements where output of one is input to other	**J.**	256
		K.	8
		L.	Memory
		M.	16

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	decoder	**B.**	serial	**C.**	over-flow
D.	low	**E.**	two's complement	**F.**	JK flip-flop
G	bus	**H.**	high	**I.**	Control Unit
J.	main	**K.**	sign and magnitude	**L.**	excitation table
M.	Counter				

4.1 An AND gate generates a high output when all its inputs are _____.

4.2 Indeterminate condition of the SR flip-flop (when S=R=1) is eliminated in _____.

4.3 In the Assembly, instruction ISZ CTR, the operand CTR refef to _____.

4.4 A table that lists the required inputs for a given change of state is _____.

4.5 Memory and CPU are connected through a _____.

4.6 Virtual memory is used to increase the apparent size of the _____ memory.

4.7 _____ interface is used to connect the processor to I/O devices that require transmission of data one bit at a time.

4.8 When the addition of two +ve numbers results in a –ve value, then _____ flag will be set.

4.9 Assembly language is _____ level programming language.

4.10 Positive and negative zeros are limitation of _____ method.

PART TWO

(Attempt any **FOUR** questions)

5.

a) Convert the following infix expression to reverse polish notation, clearly showing the steps involved.

A*B+C/D

b) Construct the truth table for 2-4 line decoder with NAND gates, and show the logic diagram.

(5+10)

6.

a) Explain the following addressing modes, with help of suitable examples.

i) Indexed addressing mode
ii) Register addressing mode
iii) Indirect addressing mode
iv) Immediate addressing mode

b) What is cycle stealing? How is data transferred by DMA?

(8+7)

7.

a) For a computer with 32 bit word size, 128 MB memory, instruction set of size 200, 16 registers,

i) What is the size of address space?
ii) What is the size of opcode?
iii) What is the size of registers?
iv) What is the size of two address, register-register instruction?

b) Simplify the following Boolean expression either algebraically or using K-Maps, and draw the logic diagram.

$$AC' + B'D + A'CD + ABCD$$

(6+9)

8.

a) Show the step-by-step multiplication process using Booth Algorithm for (+15) x (-13). Assume 5-bit registers that hold signed numbers. The multiplicant is +15.

b) A digital computer has a memory unit of 64k x 16 and a cache memory of 1k words. The cache uses direct mapping with a block size of four words.

i) How many bits are there in the tag, index, block and word fields of the address format.
ii) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit.
iii) How many blocks can the cache accommodate?

(6+9)

9. Write short notes on **any three** of the following:

a) Interrupt service routine
b) RISC vs. CISC computers
c) Asynchronous serial transfer
d) Instruction cycle of CPU
e) 2's complement method
f) Memory mapped I/O

(3x5)