Curriculum

Scheme & Syllabi

for M.Tech Course in

EMBEDDED SYSTEMS

of

Kerala Technological University

Cluster No 09 : Calicut

(With Effect from the Academic Year 2015 onwards)

Scheme of M.Tech. Programme in EMBEDDED SYSTEMS
(With Effect from the Academic Year 2015 onwards)

Semester 1 (Credits 23)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks	End Semester Exam		Total Marks	Credits
			L	T	P		Marks	Dur (h)		
1.	09EC6611	System Design using Embedded Processors	3	1	0	40	60	3	100	4
2.	09EC6621	Advanced Engineering Mathematics	3	1	0	40	60	3	100	4
3.	09EC6631	Embedded Programming	3	1	0	40	60	3	100	4
4.	09EC6641	Advanced Digital System Design	3	0	0	40	60	3	100	3
5.	09EC66x5	Elective I	3	0	0	40	60	3	100	3
6.	09EC6651	Research Methodology	0	2	0	100	0	0	100	2
7.	09EC6661	Seminar	0	0	2	100	0	0	100	2
8.	09EC6671	System Design using Embedded Processors - Laboratory	0	0	2	100	0	0	100	1
		Total	**16**	**3**	**4**	**500**	**300**		**800**	**23**
		Elective I					-			
1.	09EC6615	Electronic System Design								
2.	09EC6625	Wireless Sensor Networks								
3.	09EC6635	Advanced Data Communications								
4.	09EC6645	Software Engineering								

Semester 2 (Credits 19)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks	End Semester Exam		Total Marks	Credits
			L	T	P		Marks	Dur (h)		
1.	09EC6612	Embedded OS & RTOS	3	1	0	40	60	3	100	4
2.	09EC6622	Design of Digital Signal Processing Systems	3	0	0	40	60	3	100	3
3.	09EC6632	Product Design and Quality Management	3	0	0	40	60	3	100	3
4.	09EC66x6	Elective - II	3	0	0	40	60	3	100	3
5.	09EC66x6	Elective - III	3	0	0	40	60	3	100	3
6.	09EC6662	Mini Project	0	0	4	100	0	0	100	2
7.	09EC6672	Design of Digital Signal Processing Systems - Laboratory	0	0	2	100	0	0	100	1
		Total	**15**	**0**	**6**	**400**	**300**		**700**	**19**
		Elective II & III								
1.	09EC6616	Internet of Things **(**IoT)								
2.	09EC6626	Multimedia Compression Techniques								
3.	09EC6636	Information Security								
4.	09EC6646	ASIC & SOC								
5.	09EC6656	High Speed Digital Design								
6.	09EC6666	Embedded Applications in Power Conversion								
7.	09EC6676	Advanced Networking Technologies								
8.	09EC6686	Electronic Packaging								

L – Lecture, T- Tutorial, P – Practical

Semester 3 (Credits 14)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks		End Semester Exam		Total Marks	Credits
			L	T	P			Marks	Dur (h)		
1.	09EC76x7	Elective IV	3	0	0	40		60	3	100	3
2.	09EC76x7	Elective V	3	0	0	40		60	3	100	3
3.	09EC7663	Seminar	0	0	2	100		0	0	100	2
4.	09EC7683	Master Research Project Phase I	0	0	12	Guide	EC	0	0		6
						20	30			50	
		Total	**6**	**0**	**14**	**230**		**120**		**350**	**14**
		Elective IV & V									
1.	09EC7617	Wireless Technologies									
2.	09EC7627	Automotive Electronics									
3.	09EC7637	Mixed Signal System Design									
4.	09EC7647	Robotics and Machine Vision									
5.	09EC7657	Electronic Instrumentation Design									
6.	09EC7667	Advanced Digital Communications									
7.	09EC7677	VLSI Signal Processing									
8.	09EC7687	Cloud Computing									

Semester 4 (Credits 12)

Sl No	Course Code	Name of the Subject	Hours / Week			Internal Marks			End Semester Exam		Total Marks	Credits
			L	T	P				Marks	Dur (h)		
1.	09EC7684	Master Research Project Phase II	0	0	21	Guide	Ext expert	EC	0	0		12
						30	30	40			100	
		Total	**0**	**0**	**21**	**100**			**0**		**100**	**12**
		Grand Total				**1350**			**600**		**1950**	**68**

EC-Evaluation Committee, L – Lecture, T- Tutorial, P – Practical,

Teaching assistance of 6 hours/week in all semesters for GATE students

Examination Pattern

1. Theory Subjects

The examination pattern for all theory subjects is as given below.

Internal Continuous Assessment: 40 marks

Internal continuous assessment is in the form of periodical tests, assignments, seminars or a combination of all whichever suits best. There will be two tests per subject. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

End Semester Examination: 60 marks

2. Laboratory Subjects

The details of the internal assessment for each laboratory subject are as given below.

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

3. Seminar/ Mini Projects

Seminar shall be evaluated by the evaluation committee based on the relevance of topic, content depth and breadth, communication skill, question answering etc on the power point presentation of the topic by the student.

Mini Projects shall be evaluated by the evaluation committee based on the demonstration of the project as well as power point presentation of the same.

FIRST SEMESTER

Course No: 09EC6611

Course Title: SYSTEM DESIGN USING EMBEDDED PROCESSORS

Credits: 3-1-0: 4 Year : 2015

Pre-requisites: Nil

Objective:
The objective is to impart the concepts and architecture of Embedded systems and to make the students capable of designing Embedded systems. To achieve this, the architecture and programming of Industry popular 32-bit Microcontroller, ARM Cortex is covered in detail.

Syllabus:
Embedded Concepts, Architecture of embedded systems, ARM Architecture, Cortex-M3 Basics, Exceptions, Instruction Sets, NVIC, Interrupt Behaviour, Cortex-M3/M4 Programming, Exception Programming, Memory Protection Unit and other Cortex-M3 features, STM32L15xxx ARM Cortex M3/M4 Microcontroller Memory and Peripherals, Development & Debugging Tools.

Course Outcome:

After successful completion of the course, students should be able to:

Understand the Embedded Concepts and Architecture of Embedded Systems
Understand the architecture and programming of Industry standard 32-bit popular ARM Cortex Microcontroller
Select a proper Microcontroller for a particular application
Understand the usage of the development and debugging tools.

TEXT BOOKS:

1. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
2. Andrew N Sloss, Dominic Symes, Chris Wright, “ARM System Developer's Guide - Designing and Optimizing System Software”, 2006, Elsevier.

REFERENCES:

1. Steve Furber, “ARM System-on-Chip Architecture”, 2nd Edition, Pearson Education
2. Cortex-M series-ARM Reference Manual
3. Cortex-M3 Technical Reference Manual (TRM)
4. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
5. David Seal “ARM Architecture Reference Manual”, 2001 Addison Wesley, England; Morgan Kaufmann Publishers
6. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual

7. ARM Company Ltd. “ARM Architecture Reference Manual– ARM DDI 0100E”
8. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).
9. Ajay Deshmukh, “Microcontroller - Theory & Applications”, Tata McGraw Hill
10. Arnold. S. Berger, “Embedded Systems Design - An introduction to Processes, Tools and Techniques”, Easwer Press
11. Raj Kamal, “Microcontroller - Architecture Programming Interfacing and System Design” 1st Edition, Pearson Education
12. P.S Manoharan, P.S. Kannan, “Microcontroller based System Design”, 1st Edition, Scitech Publications

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6611 Title: **SYSTEM DESIGN USING EMBEDDED PROCESSORS** (L-T-P): 3-1-0 Credits: 4		
Modules	Hours	% marks in ESE
Module 1 **Embedded Concepts** Introduction to embedded systems, Application Areas, Categories of embedded systems, Overview of embedded system architecture, Specialties of embedded systems, recent trends in embedded systems, Architecture of embedded systems, Hardware architecture, Software architecture, Application Software, Communication Software, Development and debugging Tools. **ARM Architecture** Background of ARM Architecture, Architecture Versions, Processor Naming, Instruction Set Development, Thumb-2 and Instruction Set Architecture.	10	25
Module 2 **Overview of Cortex-M3** **Cortex-M3 Basics:** Registers, General Purpose Registers, Stack Pointer, Link Register, Program Counter, Special Registers, Operation Mode, Exceptions and Interrupts, Vector Tables, Stack Memory Operations, Reset Sequence.	7	13

Instruction Sets: Assembly Basics, Instruction List, Instruction Descriptions. **Cortex-M3 Implementation Overview:** Pipeline, Block Diagram, Bus Interfaces on Cortex-M3, I-Code Bus, D-Code Bus, System Bus, External PPB and DAP Bus.		
FIRST INTERNAL TEST		
Exceptions: Exception Types, Priority, Vector Tables, Interrupt Inputs and Pending Behavior, Fault Exceptions, Supervisor Call and Pendable Service Call. **NVIC:** Nested Vectored Interrupt Controller Overview, Basic Interrupt Configuration, Software Interrupts and SYSTICK Timer. **Interrupt Behavior:** Interrupt/Exception Sequences, Exception Exits, Nested Interrupts, Tail-Chaining Interrupts, Late Arrivals and Interrupt Latency	6	12
Module 3 **Cortex-M3/M4 Programming:** **Cortex-M3/M4 Programming:** Overview, Typical Development Flow, Using C, CMSIS (Cortex Microcontroller Software Interface Standard), Using Assembly. **Exception Programming:** Using Interrupts, Exception/Interrupt Handlers, Software Interrupts, Vector Table Relocation. **Memory Protection Unit and other Cortex-M3 features:** MPU Registers, Setting Up the MPU, Power Management**,** Multiprocessor Communication.	10	25
SECOND INTERNAL TEST		
Module 4 **Cortex-M3/M4 Microcontroller** **STM32L15xxx ARM Cortex M3/M4 Microcontroller:** Memory and Bus Architecture, Power Control, Reset and Clock Control. **STM32L15xxx Peripherals:** GPIOs, System Configuration Controller, NVIC, ADC, Comparators, GP Timers, USART. **Development & Debugging Tools:** Software and Hardware tools like Cross Assembler, Compiler, Debugger, Simulator, In-Circuit Emulator (ICE), Logic Analyzer etc.	9	25
Tutorial	14	
END SEMESTER EXAMINATION		
Total Hours	**56**	

Course No: 09EC6621

Course Title: ADVANCED ENGINEERING MATHEMATICS

Credits: 3-1-0: 4 Year : 2015

Pre-requisites: Nil

Objective:

- To understand methods of advanced engineering mathematics including advanced methods found in solving linear ordinary differential equations, matrix inversion, matrix factorization and vector spaces.
- To understand basic concept of Orthogonality, Orthogonal bases and linear transforms.
- To demonstrate knowledge of Laplace, Fourier and 'Z' transform methods in the solution of a spectrum of applications in engineering.
- To understand the importance of orthogonal and unitary transforms for various engineering applications.
- Demonstrate the application of unitary transforms for signal and image processing applications.
- To understand the basic concept of Wavelets and Wavelet Transform.

Syllabus:

Linear Algebra, Linear Equations and Matrix Algebra, Linear Transforms, Orthogonality, Digital Transforms and Arithmetic, 2D orthogonal & unitary transforms, Properties of unitary transforms, 1D and 2D- DFT, Walsh, Hadamard Transform, Haar Transform, SVD Transform, Digital Arithmetic, Wavelet Transform

Course Outcome:

After successful completion of the course, students should be able to get:

- A sound understanding of system of linear equations and ability solve them.
- A sound understanding of the Gauss elimination and ability to use it to solve linear system.
- A sound understanding of Matrix factorization, inversion and ability to solve them.
- Ability to employ Laplace and Z transform to solve linear systems.
- A sound understanding of Orthogonality, Orthogonal bases and linear transforms.
- Ability to employ linear transforms for solving signal and image processing applications.
- A sound understanding of Wavelets and Wavelet transform.

TEXT BOOKS:

1. "Linear Algebra and its Applications", David C. Lay, 3rd edition, Pearson Education (Asia) Pte. Ltd, 2005

2. Digital Arithmetic, Milos D. Ercegovac, Tomas Lang, Elsevier

REFERENCES:

1. "Fundamentals of Digital Image Processing", Anil K. Jain, PHI, New Delhi
2. Digital Signal Processing: a practical approach, Emmanuel C Ifeachor, W Barrie Jervis, Pearson Education (Singapore) Pte. Ltd., Delhi
3. Wavelet transforms-Introduction to theory and applications, Raghuveer M.Rao and Ajit S. Bapardikar, Person Education
4. Linear Algebra and its Applications, GilbertStrang.
5. Schaum's Outline for Advanced Engineering Mathematics for Engineers and Scientists , Murray R. Spiegel, MGH Book Co., New York
6. Advanced Engineering Mathematics, Erwin Kreyszing, John Wiley & Sons, NEW YORK
7. Advanced Engineering Mathematics, JAIN, R K,IYENGAR, S R K, Narosa, NEW YORK
8. Signal processing with fractals: a Wavelet - based approach, Wornell, Gregory, PH, PTR, NEW JERSEY 5. Wavelet a primer, Christian Blatter, Universities press (India) limited, Hyderabad

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6621 Title: **ADVANCED ENGINEERING MATHEMATICS** (L-T-P): 3-1-0 Credits: 4		
Modules	Hours	% marks in ESE
Module 1 : Linear Algebra Linear Equations and Matrix Algebra: Fields; system of linear equations, and its solution sets; elementary row operations and echelon forms; matrix operations; invertible matrices, LU-factorization Vector Spaces: Vector spaces; subspaces; bases ; dimension; coordinates	10	25
Module 2 : Linear Transforms Orthogonality: Orthogonal Vectors and Subspaces, Cosines and Projections onto lines, Projections and least squares, Orthogonal Bases and Gram-Schmidt orthogonalization.	6	13
FIRST INTERNAL TEST		

Linear Systems and Shift invariance, The Laplace Transform, Properties, The Fourier Transform, Properties of Fourier Transform, Fourier Transform of Sequence(Fourier Series) and its properties, Z Transform and its properties.	7	12
Module 3: Digital Transforms and Arithmetic Introduction, 2D orthogonal & unitary transforms, Properties of unitary transforms, 1D and 2D- DFT, Walsh, Hadamard Transform, Haar Transform, SVD Transform. Digital Arithmetic: Fixed and Floating point representation, IEEE 754 Floating point standards, Floating point arithmetic operations.	10	25
SECOND INTERNAL TEST		
Module 4: Wavelet Transform Wavelet Transform: Continuous: introduction, C-T wavelets, properties, inverse CWT. Discrete Harr Wavelet Transform and orthogonal wavelet decomposition using Harr Wavelets.	9	25
Tutorial	14	
END SEMESTER EXAMINATION		
Total Hours	**56**	

Course No: 09EC6631

Course Title: EMBEDDED PROGRAMMING

Credits: 3-1-0: 4 Year : 2015

Pre-requisites: Knowledge of basic C programming

Objective:

- This subject is framed to set the required background in embedded system concepts, Fundamentals of Linux OS and 'C' language for the rest of the modules.
- It aims at familiarizing the students in embedded concepts and programming in 'C'. This module covers the advanced topics in 'C' such as Memory management, Pointers, Data structures which are of high relevance in embedded software is considered in depth.
- The syllabus also covers the topic 'scripting languages for embedded systems'.

Syllabus:

Embedded OS Fundamentals, Operating System Fundamentals, Embedded Linux, GNU Tools, Embedded C Programming, Review of data types, Introduction to Embedded C, Embedded programming issues, Modelling Language for Embedded Systems, Embedded Applications using Data structures, Linear data structures– Stacks and Queues, Nonlinear structures – Trees and Graphs, Object Oriented programming basics, Scripting Languages for Embedded Systems

Course Outcome:

After successful completion of the course, students should be able to:

- Develop advanced programs in Embedded C
- Get knowledge in Embedded OS (Linux) fundamentals
- Develop programs using scripting languages

TEXT BOOKS:

1. C Programming language, Kernighan, Brian W, Ritchie, Dennis M
2. "Embedded C",Michael J. Pont, Addison Wesley

REFERENCES:

1. "Exploring C for Microcontrollers- A Hands on Approach",Jivan S. Parab, Vinod G. Shelake, Rajanish K.Kamot, and Gourish M.Naik, Springer.
2. Daniel W. Lewis, "Fundamentals of embedded software where C and assembly meet", Pearson Education, 2002.

3. Bruce Powel Douglas, “Real time UML, second edition: Developing efficient objects for embedded systems”, 3rd Edition 1999, Pearson Education. 3. Steve Heath, “Embedded system design”, Elsevier, 2003.
4. David E. Simon, “An Embedded Software Primer”, Pearson Education, 2003.
5. The Complete Reference C++, Herbert Schildt, TMH
6. C++ programming language, Bjarne Stoustrup,Addison-Wesley
7. GNU C++ For Linux, Tom Swan , Prentice Hall India
8. Object_Oriented programming in C++, Robert Lafore , Galgotia publications
9. Operating System Concepts, Peter B. Galvin, Abraham Silberschatz, Gerg Gagne, Wiley Publishers
10. GNU/LINUX Application Programming, Jones, M Tims

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6631 Title: **EMBEDDED PROGRAMMING** (L-T-P): 3-1-0 Credits: 4		
Modules	Hours	% marks in ESE
Module 1: Embedded OS Fundamentals (Linux) Introduction: Operating System Fundamentals, General Linux Architecture, Linux Kernel, Linux file systems, ROOTFS, Sysfs and Procfs, Embedded Linux: Booting Process in Linux, boot loaders, U-boot, Kernel Images, Linux File systems. GNU Tools: gcc, gdb, gprof, Makefiles	9	25
Module 2: Embedded C Programming Review of data types –scalar types-Primitive types-Enumerated types-Subranges, Structure types-character strings –arrays- Functions Introduction to Embedded C-Introduction, Data types Bit manipulation, Interfacing C with Assembly.	6	13
FIRST INTERNAL TEST		

Embedded programming issues - Reentrancy, Portability, Optimizing and testing embedded C programs. Modelling Language for Embedded Systems: Modeling and Analysis of Real-Time and Embedded systems	6	12
Module 3: Embedded Applications using Data structures Linear data structures– Stacks and Queues Iimplementation of stacks and Queues- Linked List - Implementation of linked list, Sorting, Searching, Insertion and Deletion, Nonlinear structures – Trees and Graphs Object Oriented programming basics using C++ and its relevance in Embedded systems..	12	25
SECOND INTERNAL TEST		
Module 4: Scripting Languages for Embedded Systems Shell scripting, Programming basics of Python, Comparison of scripting languages	9	25
Tutorial	14	
END SEMESTER EXAMINATION		
Total Hours	**56**	

Course No: 09EC6641

Course Title: ADVANCED DIGITAL SYSTEM DESIGN

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

To prepare students for the design of practical digital hardware systems using VHDL. This course covers the basics of digital logic circuits and design and introduces the student to the fundamentals of combination logic design and then to sequential circuits (both synchronous and asynchronous). Memory systems are also covered. Students will be provided opportunities to synthesize the designs (using both schematic capture and VHDL) for implementation in FPGAs.

Syllabus:

Introduction to Digital Design, Combinational and Sequential Circuit Design, State machine design, Design of Asynchronous Sequential Circuit, Designing with PLDs, and CPLDs. HDL, Introduction to Synthesis and Synthesis Issues

Testing, Fault Modelling and Test Generation, Test generation for combinational logic circuits, Introduction to Design for Testability. FPGAs, Logic blocks, Routing architecture, Design flow technology, Xilinx and Altera FPGA Architecture.

Course Outcome:

The students will be able to design, simulate, built and debug complex combinational and sequential circuits based on an abstract functional specification and implement the designs on FPGAs.

TEXT BOOKS:

1. Parag K. Lala, "Digital System Design using programmable Logic Devices", Prentice Hall, NJ, 1994
2. Geoff Bestock, "FPGAs and programmable LSI; A Designers Handbook", Butterworth Heinemann, 1996

REFERENCES:

1. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, “Digital Systems Testing and Testable Design”, John Wiley & Sons Inc.

2. Parag K.Lala “Fault Tolerant and Fault Testable Hardware Design” B S Publications, 2002
3. J. Bhasker, "A VHDL Primer", Addison-Weseley Longman Singapore Pte Ltd. 1992
4. Jesse H. Jenkins, "Designing with FPGAs and CPLDs", Prentice Hall, NJ,1994
5. Fundamentals of Logic Design – Charles H. Roth, 5th ed., Cengage Learning.
6. Kevin Skahill, "VHDL for Programmable Logic", Addison -Wesley, 1996
7. Z. Navabi, "VHDL Analysis and Modeling of Digital Systems", McGRAW-Hill, 1998
8. Digital Circuits and Logic Design – Samuel C. Lee , PHI
9. Smith, "Application Specific Integrated Circuits", Addison-Wesley, 1997
10. P.K. Lala, “Digital Circuit Testing and Testability”, Academic Press, 2002

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6641 Title: **ADVANCED DIGITAL SYSTEM DESIGN** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 **Introduction to Digital Design** Combinational Circuit Design, Synchronous Sequential Circuit Design - Mealy and Moore model, State machine design, Analysis of Synchronous sequential circuit, State equivalence, State Assignment and Reduction, Analysis of Asynchronous Sequential Circuit, flow table reduction, races, state assignment, Design of Asynchronous Sequential Circuit, Designing with PLDs – Overview of PLDs – ROMs, EPROMs – PLA – PAL - Gate Arrays – CPLDs and FPGAs, Designing with ROMs - Programmable Logic Arrays - Programmable Array logic, PAL series 16 & 22 – PAL22V10 - Design examples.	12	25
Module 2 **VHDL** Basics – Introduction to HDL – Behavioral modeling – Data flow modeling – Structural modeling – Basic language elements – Entity – Architecture – Configurations – Subprograms & operator overloading – Packages and libraries – Test Bench – Advanced Features – Model simulation	7	13

FIRST INTERNAL TEST		
Realization of combinational and sequential circuits using HDL – Registers – Flip flops – counters – Shift registers –Multiplexers – sequential machine – Multiplier – Divider, Introduction to Synthesis and Synthesis Issues.	5	12
Module 3 **Testing, Fault Modelling And Test Generation –** Introduction to testing – Faults in Digital Circuits – Modelling of faults – Logical Fault Models – Fault detection – Fault Location – Fault dominance – Logic simulation – Test generation for combinational logic circuits – Testable combinational logic circuit design, Introduction to Design for Testability, BST	8	25
SECOND INTERNAL TEST		
Module 4 **FPGA** - FPGAs - Logic blocks, Routing architecture, Design flow technology - mapping for FPGAs, Xilinx FPGA Architecture, Xilinx XC4000 - ALTERA's FLEX 8000, Design flow for FPGA Design, Case studies: Virtex II Pro.	10	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

09EC66x5 - ELECTIVE I

Course No: 09EC6615

Course Title: ELECTRONIC SYSTEM DESIGN

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

To give the student a foundation in

- practical analog, digital and mixed signal circuit design issues and techniques
- electromagnetic compatibility design issues
- packaging and thermal aspects in enclosure design

Syllabus:

Practical Analog & Mixed Signal Circuit Design Issues and Techniques, Op amps, ADCs and DACs, Power supplies, Practical Logic Circuit Design Issues and Techniques, Design for testability, Electromagnetic Compatibility (EMC), Cabling of Electronic Systems, Grounding of Electronic Systems, Balancing & Filtering in Electronic Systems, Protection Against Electrostatic Discharges (ESD), Packaging & Enclosures of Electronic System, Cooling in/of Electronic System.

Course Outcome:

After successful completion of the course, the student will have demonstrated an ability to apply the practical design concepts in analog, digital and mixed signal circuits; design concepts of EMC and ESD in PCB and system design; the design concepts of packaging and enclosure design to take care of environmental and thermal requirements.

TEXT BOOKS:

1. Electronic Instrument Design, 1st edition; by: Kim R.Fowler; Oxford University Press.
2. Noise Reduction Techniques in Electronic Systems, 2nd edition; by: Henry W.Ott; John Wiley & Sons.
3. Digital Design Principles& Practices, 3rd edition by: John F. Wakerly; Prentice Hall International, Inc.

REFERENCES:

1. Operational Amplifiers and linear integrated circuits, 3rd edition by: Robert F. Coughlin; Prentice Hall International, Inc
2. Intuitive Analog circuit design by: Mark.T Thompson; Published by Elsevier
3. Printed Circuit Boards - Design & Technology, 1st edition; by: W Bosshart; Tata McGraw Hill.

4. A Designer's Guide to Instrumentation Amplifiers; by: Charles Kitchin and Lew Counts; Seminar Materials @ http://www.analog.com
5. Errors and Error Budget Analysis in Instrumentation Amplifier Applications; by: Eamon Nash; Application note AN-539@ http://www.analog.com
6. Practical Analog Design Techniques; by: Adolofo Garcia and Wes Freeman; Seminar Materials@ http://www.analog.com
7. Selecting An A/D Converter; by:Larry Gaddy; Application bulletin @ http://www.Ti.com
8. Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies; Application note SDAA011A@ http://www.Ti.com
9. JTAG/IEEE 1149.1 deigns considerations; Application note SCTA029@ http://www.Ti.com
10. Live Insertion; Application note SDYA012@ http://www.Ti.com
11. PCB Design Guidelines For Reduced EMI; Application note SZZA009@ http://www.Ti.com

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6615 Title: **ELECTRONIC SYSTEM DESIGN** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Practical Analog & Mixed Signal Circuit Design Issues and Techniques: Passive components: Understanding and interpreting data sheets and specifications of various passive and active components, non-ideal behavior of passive components,. Op amps: DC performance of op amps: Bias, offset and drift. AC Performance of operational amplifiers: band width, slew rate and noise. Properties of a high quality instrumentation amplifier. Design issues affecting dc accuracy & error budget analysis in instrumentation amplifier applications. Isolation amplifier basics. Active filers: design of low pass, high pass and band pass filters. ADCs and DACs: Characteristics, interfacing to microcontrollers. Selecting an ADC.	10	25

Power supplies: Characteristics, design of full wave bridge regulated power supply. Circuit layout and grounding in mixed signal system.		
Module 2 Practical Logic Circuit Design Issues and Techniques: Understanding and interpreting data sheets & specifications of various CMOS& BiCMOS family Logic devices. Electrical behavior (steady state & dynamic) of CMOS& BiCMOS family logic devices.	6	13
FIRST INTERNAL TEST		
Benefits and issues on migration of 5-volt and 3.3 volt logic to lower voltage supplies. CMOS/TTL Interfacing Basic design considerations for live insertion. JTAG/IEEE 1149.1 design considerations. Design for testability, Estimating digital system reliability. Digital circuit layout and grounding. PCB design guidelines for reduced EMI.	6	12
Module 3 Electromagnetic Compatibility (EMC): Designing for (EMC), EMC regulations, typical noise path, methods of noise coupling, methods of reducing interference in electronic systems. Cabling of Electronic Systems: Capacitive coupling, effect of shield on capacitive coupling, inductive coupling, effect of shield on inductive coupling, effect of shield on magnetic coupling, magnetic coupling between shield and inner conductor, shielding to prevent magnetic radiation, shielding a receptor against magnetic fields, coaxial cable versus shielded twisted pair, ribbon cables. Grounding of Electronic Systems: Safety grounds, signal grounds, single-point ground systems, multipoint-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies.	10	25
SECOND INTERNAL TEST		
Module 4 Balancing & Filtering in Electronic Systems: Balancing, power line filtering, power supply decoupling, decoupling filters, high frequency filtering, system bandwidth. Protection Against Electrostatic Discharges (ESD):	10	25

Static generation, human body model, static discharge, ESD protection in equipment design, software and ESD protection, ESD versus EMC. Packaging & Enclosures of Electronic System: Effect of environmental factors on electronic system (environmental specifications), nature of environment and safety measures. Packaging's influence and its factors. Cooling in/of Electronic System: Heat transfer, approach to thermal management, mechanisms for cooling, operating range, basic thermal calculations, cooling choices, heat sink selection.		
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6625

Course Title: WIRELESS SENSOR NETWORKS

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- This subject is framed to set the required background in wireless communication. Being the backbone for all the IT based developments; Wireless Sensor Network has seen tremendous growth in the past decade. There are new techniques and protocols emerging from time-to-time to cater the requirements of this rapidly growing area.
- The subject will cover fundamentals and advanced topics of Wireless Sensor Networks.
- The treatment would look at current and upcoming wireless sensor networks, protocols for various automation applications.

Syllabus:

Issues in Ad Hoc Wireless Networks**,** Sensor Networks Comparison with Adhoc wireless networks-Challenges for WSNs, Enabling Technologies for Wireless Sensor Networks, Sensor Network Architecture, Gateway Concepts, MAC Protocols MAC Protocols for Sensor Networks, Routing Gossiping and Agent based Unicast Forwarding, Energy Efficient Unicast-Broadcast and Multicast Geographic Routing

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the different wireless sensor network basics and protocols .
- Understand the basics of wireless sensor network development.

TEXT BOOKS:

1. Holger Karl and Andreas Wiilig, “Protocols and Architectures for Wireless Sensor Networks” John Wiley & Sons Limited 2008.
2. I.F .Akyildiz and Weillian, “A Survey on Sensor Networks”,IEEE Communication Magazine, August 2007.

REFERENCES:

1. Wilson , “Sensor Technology hand book,” Elsevier publications 2005.
2. Anna Hac “Wireless Sensor Networks Design,” John Wiley& Sons Limited Publications 2003.

3. C.Siva Ram Murthy and B.S.Manoj "Ad Hoc Wireless Networks," Pearson Edition 2005.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6625 Title: **WIRELESS SENSOR NETWORKS** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Issues in Ad Hoc Wireless Networks: Medium Acces Scheme-Routing-Multicasting-Transport Layer Protocols-Self Organization-Security-Addressing and Service Discovery Energy management-Scalability-Deployment Considerations, Ad Hoc Wireless Internet. Sensor Networks Comparison with Adhoc wireless networks-Challenges for WSNs - Difference between sensor networks and Traditional sensor networks –Types of Applications –Enabling Technologies for Wireless Sensor Networks –Single Node Architectures –Hardware Components – Energy Consumption of Sensor Nodes, Issues in Designing a Multicast Routing Protocol. OS for WSN.	12	25
Module 2 Sensor Network Architecture Data Dissemination-Flooding and Gossiping-Data gathering Sensor Network Scenarios –Optimization Goals and Figures of Merit	6	13
FIRST INTERNAL TEST		
Design Principles for WSNs- Gateway Concepts – Need for gateway – WSN to Internet Communication – Internet to WSN Communication –WSN Tunneling.	6	12
Module 3 MAC Protocols MAC Protocols for Sensor Networks -Location Discovery-Quality of Sensor Networks-Evolving Standards-Other Issues- Low duty cycle and wake up concepts- The IEEE 802.15.4 MAC Protocols Energy	9	25

Efficiency -Geographic Routing Mobile nodes		
SECOND INTERNAL TEST		
Module 4 Routing Gossiping and Agent based Unicast Forwarding-Energy Efficient Unicast-Broadcast and Multicast Geographic Routing-Mobile nodes-Security-Application Specific Support - Target detection and tracking-Contour/ edge detection-Field Sampling.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC66 35

Course Title: ADVANCED DATA COMMUNICATIONS

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- The objective of the course is to provide understanding of advanced concepts of data communication.
- Along with basics it also covers the protocols like USART, USB, I2C , CAN etc.

Syllabus:

Digital Modulation Schemes, Multiplexing, Basic Concepts of Data Communications, Data Communication Networks, Protocols and Standards, Error Correction, Error Control Data Link Protocols, Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation Polling.

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the concepts and technologies used in the data communication domain.
- Understand the various protocols used in the various data communication applications.
- Get knowledge about latest trends in the data communication field

TEXT BOOKS:

1. Data Communication and Computer Networking - B. A.Forouzan, 2nd Ed., 2003, TMH.
2. Advanced Electronic Communication Systems - W. Tomasi, 5th Ed., 2008, PEI

REFERENCES:

1. Data and Computer Communications - William Stallings, 8th Ed., 2007, PHI.
2. Data Communication and Tele Processing Systems -T. Housely, 2nd Ed, 2008, BSP.
3. Data Communications and Computer Networks- Brijendra Singh, 2nd Ed., 2005, PHI.

4. Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6635 Title: **ADVANCED DATA COMMUNICATIONS** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1: Digital Modulation Schemes: BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery. Multiplexing: Frequency Division Multiplexing (FDM), Time Division Multiplexing (TDM), Multiplexing Application, SMDS Switching: Circuit Switching, Packet Switching, Message Switching. Networking and Interfacing Devices: Repeaters, Bridges, Routers, Gateway, Other Devices.	11	25
Module 2: Basic Concepts of Data Communications, Interfaces and Modems: Data Communication Networks, Protocols and Standards, CAN, UART, USB, I2C, I2S, Line Configuration, Topology, Transmission Modes,	6	13
FIRST INTERNAL TEST		
Digital Data Transmission, DTE-DCE interface, Categories of Networks – TCP/IP Protocol suite and Comparison with OSI model.IPV4 and IPV6.	6	12
Module 3 Error Correction: Types of Errors, Vertical Redundancy Check (VRC), LRC, CRC, Checksum, Error Correction using Hamming code Data Link Control: Line Discipline, Flow Control, Error Control Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocols,	10	25

Bit-Oriented Protocol, Link Access Procedures.		
SECOND INTERNAL TEST		
Module 4 Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- ReservationPolling- Token Passing, Channelization, Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), Code - Division Multiple Access (CDMA), OFDM and OFDMA.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6645

Course Title: SOFTWARE ENGINEERING

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- To explore the basics and goals of software Engineering
- To discuss various types of software testing and its techniques
- To list out various tools which can be used for automating the testing process
- To introduce various software quality standards for establishing quality environment
- To discuss various methods and evaluation procedures for improving the quality Models

Syllabus:

Software Process, Requirements Engineering Processes, Architectural Design, Object-oriented Design, Real-time Software Design, User Interface Design, Verification and Validation, Software Testing, Software Maintenance, Software Cost Estimation, Software Project Management, Process Improvement

Course Outcome:

After successful completion of the course, students should be able to:

- Compare and pick out the right type of software testing process for any given real world problem
- Carry out the software testing process in efficient way
- Establish a quality environment as specified in standards for developing quality software
- Analyze and improve the quality procedures based on the past experience

TEXT BOOKS:

1. R. S. Pressman, *Software Engineering*, 6/e, McGraw Hill, 2002.

REFERENCES:

1. Ian Sommerville, *Software Engineering*, 6/e, Pearson Education Asia, 2001.
2. Shari Pfleeger, Software Engineering:Theory and Practice, Pearson Education 2001.
3. P. Jalote, *An Integrated Approach to Software Engineering*, Narosa, 1993.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6645 Title: **SOFTWARE ENGINEERING** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 - Introduction What is Software Engineering, The Software Process: Software life cycle models Software Requirements: Functional and non-functional requirements, user requirements, system requirements, SRS. Requirements Engineering Processes: Feasibility studies, elicitation and analysis, validation, management. System Models: Content model, Data model, Behavioral model, Object Model	10	25
Module 2 - Architectural Design System structuring, control models, modular decomposition, domain-specific architectures, distributed systems architecture. Object-oriented Design: Objects and classes, Object oriented design using UML.	6	13
FIRST INTERNAL TEST		
Real-time Software Design: System design, real time executives. Design with Reuse: Component-based development, application families, designs patterns. User Interface Design: Design principles, user interaction, information presentation, user support, interface evaluation.	6	12
Module 3 - Implementation and Testing Choice of programming languages Verification and Validation, Software Testing: Unit testing, Integration Testing, Validation testing, Systems testing Software Maintenance: Legacy systems, software change, software re-engineering, Reverse Engineering.	10	25
SECOND INTERNAL TEST		
Module 4	10	25

Software Project Management: Project planning, scheduling, risk management.. Software Cost Estimation: Productivity estimation techniques, algorithmic cost modeling, project duration and staffing. Process Improvement: Process and product quality, process analysis and modeling, process measurement, process CMM.		
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6651

Course Title: RESEARCH METHODOLOGY

Credits: 0-2-0: 2 Year : 2015

Pre-requisites: Nil

Objective:

- To give students an insight into the steps to be followed in doing a research
- To provide an idea about technical report writing

Syllabus:

Introduction to Research Methodology; Formulating a Research Problem; Conceptualising a research design; Methods of Data Collection; Processing and Analysis of Data; Writing a Research Report; Ethical issues related to publishing; A study of the use of the following tools like Matlab and LaTeX.

Course Outcome:
Students who successfully complete this course will have clear understanding about the steps to be followed in doing research.

Text Books:

1. Ranjit Kumar, "Research Methodology: A Step-by-step Guide for Beginners", Pearson, Second Edition
2. Kothari, C.R, "Research Methodology : Methods and Techniques", New age International publishers

Reference Books:

1. Sanjit K. Mitra, "Digital Signal Processing Laboratory Using MATLAB" , Mcgraw-Hill College, ISBN-13: 978-0073108582
2. Rudra Pratap, "Getting Started with MATLAB: Version 6: A Quick Introduction for Scientists and Engineers", 2001, Oxford University Press
3. Wayne Goddard and Stuart Melville, "Research Methodology : An Introduction", 2nd Edition, 2001, Juta & Co Ltd

Internal continuous assessment: 100 marks

Internal continuous assessment :
Test 1- 30 marks
Test 2- 30 marks
Assignment/Tutorial-40 marks
Total-100marks

COURSE PLAN:

Course No: 09EC6651 Title: **RESEARCH METHODOLOGY** (L-T-P): 0-2-0 Credits: 2		
Modules	Hours	% marks in ESE
Module 1 **Research Methodology: An Introduction** Meaning of Research, Objectives of Research, Motivation in Research, Applications of Research, Definition of Research, Characteristics of Research, Types of Research, Steps in Research Process **Formulating a Research Problem** Reviewing the Literature, Formulating a Research Problem, Identifying Variables, Constructing Hypothesis	7	25
Module 2 **Conceptualising a research design** Definition of a Research Design, Need for Research Design, Functions of Research Design, Features of a Good Design **Methods of Data Collection** Collection of Primary Data, Observation Method, Interview Method Collection of Data through Questionnaires, Collection of Data through Schedules	7	25
FIRST INTERNAL TEST		
Module 3 **Processing and Analysis of Data** Processing Operations, Elements/Types of Analysis, Statistics in Research, Measures of Central Tendency, Measures of Dispersion, Measures of Asymmetry (Skewness) **Writing a Research Report** Research writing in general, Referencing, Writing a Bibliography Developing an outline, Writing about a variable	7	25
Module 4 Interpretation of Data and Paper Writing – Layout of a Research Paper, Journals in Computer Science, Impact factor of Journals, When and where to publish ? Ethical issues related to publishing, Plagiarism and Self-Plagiarism **A study of the use of the following tools** Matlab / Simulink, LaTeX/ MS Office	7	25
SECOND INTERNAL TEST		
Total Hours	**28**	

Course No: 09EC6661

Course Title: SEMINAR

Credits: 0-0-2: 2 Year : 2015

Pre-requisites: Nil

Objective:
To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.

Syllabus:

Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 15 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students.

Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

Course Outcome:

After successful completion of the seminar, students should get exposed to new areas of technology and their communication, presentation skills etc. shall be improved. They shall be ready for technical paper writing and presentation.

Internal continuous assessment: 100 marks

Subject Relevance	:	10 marks
Concept/ Knowledge in the topic	:	20 marks
Presentation	:	40 marks
Report	:	30 marks
Total marks	:	**100 marks**

Course No: 09EC6671

Course Title: SYSTEM DESIGN USING EMBEDDED PROCESSORS – LABORATORY

Credits: 0-0-2: 1 Year : 2015

Pre-requisites: Nil

Objective:

To make the students familiar with the programming of 32-bit Microcontrollers and also to make them interface to the external embedded world for data acquisition etc.

Syllabus:

ARM Assembly Programming, Embedded C Programming on ARM Cortex M3/M4 Microcontroller, ARM Cortex M3/M4 Programming with CMSIS, Peripheral Interfacing

Course Outcome:

After successful completion of the lab, students will be capable of programming and interfacing details of building Microcontrollers based Embedded Systems.

REFERENCES:

1. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK.
2. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010.
3. David Seal "ARM Architecture Reference Manual", 2001 Addison Wesley, England; Morgan Kaufmann Publishers
4. Andrew N Sloss, Dominic Symes, Chris Wright, "ARM System Developer's Guide - Designing and Optimizing System Software", 2006, Elsevier.
5. Steve Furber, "ARM System-on-Chip Architecture", 2nd Edition, Pearson Education.
6. Cortex-M series-ARM Reference Manual
7. Cortex-M3 Technical Reference Manual (TRM)
8. ARM Company Ltd. "ARM Architecture Reference Manual– ARM DDI 0100E"
9. STM32L152xx ARM Cortex M3 Microcontroller Reference Manual
10. ARM v7-M Architecture Reference Manual (ARM v7-M ARM).

Internal Continuous Assessment: 100 marks

Mid Term Internal Test	40 Marks

Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

COURSE PLAN:

Course No: 09EC6671 Title: **SYSTEM DESIGN USING EMBEDDED PROCESSORS –LABORATORY** (L-T-P): 0-0-2 Credits: 1		Hours	% marks in ESE
	Module 1 – ARM Assembly Programming	7	25
1.	Write a program to add two 32-bit numbers stored in r0 and r1 registers and write the result to r2. The result is stored to a memory location. a) Run the program with breakpoint and verify the result b) Run the program with stepping and verify the content of registers at each stage		
2.	For the following values of *a* and *b*, predict the values of the N, Z, V, and C flags produced by performing the operation *a* + *b*. Load these values into two ARM registers and modify the program created in above question1 to perform an addition of the two registers. Using the debugger, record the flags after each addition and compare those results with your predictions. Values of a => 1) 0xFFFF0000 2) 0xFFFFFFFF 3) 0x67654321 Values of b => 1) + 0x87654321 2) + 0x12345678 3)+ 0x23110000		
3.	Write a program to multiply two 16-bit numbers stored in r0 and r1 registers and write the result to r3. Put 0xFFFFFFFF and 0x80000000 into the source registers and verify the result.		
4.	Write an ARM code to implement the following register swap algorithm using only two registers. a) Using arithmetic instructions b) Using logical instructions		
5.	Write ARM assembly to perform the function of absolute value. Register r0 contains the initial value, and r1 contains the absolute value.		
6.	Write ARM assembly to perform the function of division. Registers r1 and r2 contain the dividend and divisor, r3 contains the quotient, and r5 contains the remainder.		
7.	Write ARM assembly to perform the following array assignment in C: for (i = 0; i <= 10; i++) {a[i] = b[i] + c;}		

	Assume that r3 contains *i*, r4 contains *c*, the starting address of array *a* is in r1, and the starting address of array *b* is in r2.		
	Module 2 - Embedded C Programming on ARM Cortex M3/M4 Microcontroller	7	25
1. 2. 3. 4. 5.	Write a program to turn on green LED (Port B.6) and Blue LED (Port B.7) on STM32L-Discovery by configuring GPIO. Write a program to toggle green LED (Port B.6) and Blue LED (Port B.7) on STM32L-Discovery by configuring GPIO and using software delays. Write a program to toggle Blue LED (Port B.6) at a rate of 1 sec. Use Timer3 in polling method for delay generation. Transmit a string "Programming with ARM Cortex" to PC by configuring the registers of USART2. Use polling method. Transmit a string "Programming with ARM Cortex" to PC by configuring the registers of USART3. Use polling method.		
	FIRST INTERNAL TEST		
	Module 3 - ARM Cortex M3/M4 Programming with CMSIS	6	25
1. 2. 3. 4. 5. 6. 7. 8.	Write a program to toggle the LEDs at the rate of 1 sec using standard peripheral library. Use Timer3 for Delay. Transmit a string "Programming with ARM Cortex" to PC by using standard peripheral library with the help of USART3. Use polling method. Receive the data send by PC, compare it with threshold and switch on the Green LED if below threshold and Red LED if above. Write a program to read the analog input connected to ADC and compare with threshold so as to control the Digital outputs (LEDs). Use standard peripheral library and interrupt method. Write a program to toggle Blue LED (Port B.6) at a rate of 1 sec using Timer2 in interrupt configuration. Write a program to toggle Blue LED (Port B.6) at a rate of 1 sec using Timer3in interrupt configuration. Transmit a data to PC by using standard peripheral library with USART1. Use interrupts method. Receive a data sent by PC by using standard peripheral library with USART1. Use interrupts method.		
	Module 4 - ARM Cortex M3/M4 Peripherals	8	25

1. **Design of a real-time data acquisition & control system using the STM32Lxx ARM Cortex M3 Microcontroller**

It is required to monitor and control the temperature in a boiler which ranges from 0°C to 100°C every **1second** using the STM32Lxx ARM Cortex M3 Microcontroller. The temperature has to be kept at a set-point of 50°C ± 2°C. The temperature is measured through an RTD sensor and is transmitted through a 4-20 mA two wire transmitter. The 4-20mA is converted to 1 to 5V by 250 ohm terminating resistor. 1 to 5V is available at the analog input port. 1V corresponds to 0°C and 5V corresponds to 100°C. An ON/OFF relay connected to A PIO Port bit is used to control the heater element. A PC is used as the monitoring and control station.

Read the data through ADC and send the data from 0V to 5V in steps of 0.1V. The same has to be repeated after reaching the maximum value of 5V.

1. The temperature has to be sent to the PC every 1 second in the following protocol format and the same has to be displayed using the LAS software in WISE-96 on the PC.

STX	**MSL**	**CMD**	**SCMD**	**DATA_LO**	**DATA_HI**	**ET**
byte 1	byte 2	byte 3	byte 4	byte 5	byte 6	byt

STX	:	Start of Text	02H
MSL	:	Message length, in bytes	
CMD	:	Command byte	90H
SCMD	:	Sub-command byte	00H (Channel no)
DATA_LO	:	Lower byte of data word	
DATA_HI	:	Upper byte of data word	
ETX	:	End of Text	03H

2. Provision should be given for receiving the set-point value of temperature from the PC, and the set point is to be framed in the above protocol format.
3. If the transmitter is switched off or if it sends invalid data, i.e, below 4mA, an error message packet similar to the above one with CMD byte set to 95H should be send to the PC, instead of the data packet.

   Hint: Use a Trimpot to apply the voltage. Use an LED to display the ON/OFF status. ON/OFF control strategy can be used for controlling the power supplied to the heater.

SECOND INTERNAL TEST

Total Hours 28

Software used: Keil Microvision IDE, 'C' Compiler and Assembler for ARM.

Platforms used: PC, STM32L15xxx ARM Cortex M3/M4 Microcontroller Discovery Kits

SECOND SEMESTER

Course No: 09EC6612

Course Title: EMBEDDED OS & RTOS

Credits: 3-1-0: 4 Year : 2015

Pre-requisites: Nil

Objective:

- The objective of the subject is to provide understanding of the techniques essential to the design and implementation of device drivers and kernel internals of embedded operating systems.
- This syllabus provides the students with an understanding of the aspects of the Real-time systems and Real-time Operating Systems and to provide an understanding of the techniques essential to the design and implementation of real-time embedded systems.

Syllabus:

Embedded OS Internals, Overview of POSIX APIs, Kernel, Linux Device Drivers, Basics of RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Realtime scheduling, Task Creation, Intertask Communication, I/O Systems, Cross compilers, debugging Techniques, Creation of binaries & porting stages for Embedded Development board.

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the Embedded Real Time software that is needed to run embedded systems
- Understand the open source RTOS and their usage.
- Understand the VxWorks RTOS and realtime application programming with it.
- Build device driver and kernel internal for Embedded OS & RTOS.

TEXT BOOKS:

1. Essential Linux Device Drivers, Venkateswaran Sreekrishnan
2. Writing Linux Device Drivers: A Guide with Exercises, J. Cooperstein
3. Real Time Concepts for Embedded Systems – Qing Li, Elsevier

REFERENCES:

1. Embedded Systems Architecture Programming and Design: Raj Kamal, Tata McGraw Hill

2. Embedded/Real Time Systems Concepts, Design and Programming Black Book, Prasad, KVK
3. Software Design for Real-Time Systems: Cooling, J E Proceedings of 17the IEEE Real-Time Systems Symposium December 4-6, 1996 Washington, DC: IEEE Computer Society
4. Real-time Systems – Jane Liu, PH 2000
5. Real-Time Systems Design and Analysis : An Engineer's Handbook: Laplante, Phillip A
6. Structured Development for Real - Time Systems V1 : Introduction and Tools: Ward, Paul T & Mellor, Stephen J
7. Structured Development for Real - Time Systems V2 : Essential Modeling Techniques: Ward, Paul T & Mellor, Stephen J
8. Structured Development for Real - Time Systems V3 : Implementation Modeling Techniques: Ward, Paul T & Mellor, Stephen J
9. Embedded Software Primer: Simon, David E.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6612 Title: **EMBEDDED OS & RTOS** (L-T-P): 3-1-0 Credits: 4		
Modules	Hours	% marks in ESE
Module 1 – Embedded OS (Linux) Internals Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication – Semaphore, Pipes, FIFO, Shared Memory Kernel: Structure, Kernel Module Programming Schedulers and types of scheduling. Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network	11	25

Module 2 – Open source RTOS Basics of RTOS: Real-time concepts, Hard Real time and Soft Real-time, Differences between General Purpose OS & RTOS, Basic architecture of an RTOS, Scheduling Systems, Inter-process communication, Performance Matric in scheduling models, Interrupt management in RTOS environment, Memory management, File systems, I/O Systems, Advantage and disadvantage of RTOS. POSIX standards, RTOS Issues – Selecting a Real Time Operating System, RTOS comparative study.	6	13
FIRST INTERNAL TEST		
Converting a normal Linux kernel to real time kernel, Xenomai basics. Overview of Open source RTOS for Embedded systems (Free RTOS/ Chibios-RT) and application development.	6	12
Module 3 – VxWorks / Free RTOS **VxWorks/ Free RTOS** Scheduling and Task Management – Realtime scheduling, Task Creation, Intertask Communication, Pipes, Semaphore, Message Queue, Signals, Sockets, Interrupts I/O Systems – General Architecture, Device Driver Studies, Driver Module explanation, Implementation of Device Driver for a peripheral	10	25
SECOND INTERNAL TEST		
Module 4 – Case study Cross compilers, debugging Techniques, Creation of binaries **& porting stages for Embedded Development board (Beagle Bone Black, Rpi or similar),** Porting an Embedded OS/ RTOS to a target board ().Testing a real time application on the board	9	25
Tutorial	14	
END SEMESTER EXAMINATION		
Total Hours	**56**	

Course No: 09EC6622

Course Title: DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- To introduce the students to practically implementable DSP algorithms

Syllabus:

Introduction to Digital Signal Processing, Signals and Filtering, Architecture of ARM Cortex M3/M4 Processor, FIR Digital filter design, Frequency Domain,
Fourier Transform, DFT, FFT, Real-time Implementation – FIR Filter, FFT, DTMF, FPGA Technology, Multiply Accumulator (MAC) and Sum of Product

Course Outcome:

After successful completion of the course, students should be able to:

- Understand implement the standard DSP algorithms.

TEXT BOOKS:

1. Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1st Edition; by: Naim Dahnoun
2. The Definitive Guide to the ARM Cortex-M3, Joseph Yiu, Second Edition, Elsevier Inc. 2010

REFERENCES:

1. Digital Signal Processing: A System Design Approach, 1st Edition; by: David J Defatta J, Lucas Joseph G & Hodkiss William S; John Wiley
2. Digital Signal Processing with Field Programmable Gate Arrays: 2nd Edition, by: U. Meyer – Base, Springer
3. Digital Signal Processing, Third Edition, Sanjit K. Mitra, Tata McGRWA Hill
4. Digital Signal Processing – A Practical Guide for Engineers and Scientists, Steven W Smith, Elsevier
5. Digital Signal Processing - A Student Guide, 1st Edition; by: T.J. Terrel and Lik-Kwan Shark; Macmillan Press; Ltd.
6. Sanjit K. Mitra, “Digital Signal Processing Laboratory Using MATLAB” , Mcgraw-Hill College, ISBN-13: 978-0073108582
7. Sen M.Kuo , Woon-Seng S. Gan, *Digal Signal Processors: Architectures, Implementations, and Applications* Prentice Hall 2004.
8. Keshab K. Parhi, *VLSI Signal Processing Systems, Design and Implementation*, John Wiley & Sons,1999.

9. Digital Signal Processing, 1st Edition; by: Oppenheim A.V and Schafer R.W; PH
10. Digital Signal Processing Laboratory, B. Preetham Kumar, Taylor & Francis, CCS DSP Applications
11. Digital Processing of Speech Signals, 1st Edition; by: L.R. Rabiner and Schafer R.W; PH
12. A Practical Approach to Digital Signal Processing, by: K. Padmanabhan, S. Ananthi & R.Vijayarajeswaran; New Age International Publishers
13. Digital Signal Processing, 1st Edition; by: P Ramesh Babu,

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6622 Title: **DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Introduction to Digital Signal Processing Signals in Time and Frequency Domains Signals and Filtering Architecture of ARM Cortex M3/M4 Processor. ADC/ DAC Interfacing to ARM Cortex M3/M4 Processor Introduction to MATLAB and SIMULINK	10	25
Module 2 Filter Design: FIR Digital filter design. Frequency Domain Fourier Transform: DFT, FFT	7	13
FIRST INTERNAL TEST		
DTMF, Spectral Analysis	6	12

Module 3 Real-time Implementation: Real-time Implementation of FIR Digital filter using ARM Cortex M3/M4 Processor. Real-time Implementation of Fast Fourier Transform applications using ARM Cortex M3/M4 Processor. Implementation of DTMF Tone Generation and Detection ARM Cortex M3/M4 Processor.	10	25
SECOND INTERNAL TEST		
Module 4 FPGA Technology DSP Technology Requirements Design implementation Multiply Accumulator (MAC) and Sum of Product (SOP) Implementation of Serial/Parallel Convolver using FPGAs FPGA Based DSP System Design FIR filters FIR Theory Designing FIR filters Direct Window Design method Constant Coefficient FIR Design Direct FIR Design Cooley-Tukey FFT Algorithm implementation using FPGA	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6632

Course Title: PRODUCT DESIGN & QUALITY MANAGEMENT

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

To give the Student:-

- A foundation in product development process
- A foundation in Quality principles and tools
- Practice in the application of product development process and quality concepts in real life scenario

Syllabus:

Product Design and Development, Quality Management Principles, Quality Management Tools.

Course Outcome:

After successful completion of the course, students should be able to:

Students who successfully complete this course will have demonstrated an ability to understand the product development process as adopted in industry; apply the tools and techniques for product development; apply the quality principles and tools for continuous process improvement and problem solving

TEXT BOOKS:

1. Total Quality Management, Second edition By: Dale H. Besterfield, Pearson Education Asia
2. Product Design & Development; Third edition By: Karl T Ulrich & Steven D Eppinger; Mc Graw Hill

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6632 Title: **PRODUCT DESIGN & QUALITY MANAGEMENT** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 - Product Design and Development: I Development processes, Identifying customer needs, Establishing product specifications, Concept generation, Concept selection, Product architecture, Industrial design.	10	25
Module 2 - Product Design and Development: II Design for Manufacturing, Prototyping, Robust Design, Patents and Intellectual property	7	13
FIRST INTERNAL TEST		
Product Development Economics, Managing Product Development Projects.	6	12
Module 3 - Total Quality Management I Principles and Practices: Definition of quality, Customer satisfaction and Continuous improvement. **Tools and Techniques:** Statistical Process Control, Quality Systems, Bench Marking.	10	25
SECOND INTERNAL TEST		
Module 4 - Total Quality Management II Quality Function Deployment, Product Liability, Failure Mode and Effect Analysis, Management Tools.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

09EC66x6 - ELECTIVE II
&
09EC66x6 - ELECTIVE III

Course No: 09EC6616

Course Title: INTERNET OF THINGS (IoT)

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

Main objective of the course is to introduce emerging technological options, platforms and case studies of IoT implementation in home & city automation (smart homes and cities), Industrial Internet, healthcare, Govt., Mobile Cellular and other areas.

Syllabus:

The IoT Networking Core, Internet/Web and Networking Basics, IoT Platform overview, IoT Architecture and Applications, Security aspects in IoT, IoT Application Protocols, Back-end Application Design, Case Study & advanced IoT Applications.

Course Outcome:

After successful completion of the course, students should be able to:

- articulate the main concepts, key technologies, strengths, and limitations of cloud computing and the possible applications for state-of-the-art Internet of things
- identify the architecture and infrastructure of IoT.
- explain the core issues of IoT such as security, privacy, and interoperability.
- choose the appropriate technologies, algorithms, and approaches for the related issues.
- identify problems, and explain, analyze, and evaluate various IoT solutions.
- provide the appropriate IoT solutions and recommendations according to the applications used.
- attempt to generate new ideas and innovations in IoT.

TEXT BOOKS:

1. 6LoWPAN: The Wireless Embedded Internet, Zach Shelby, Carsten Bormann, Wiley
2. Internet of Things: Converging Technologies for Smart Environments and Integrated Ecosystems, Dr. Ovidiu Vermesan, Dr. Peter Friess, River Publishers

REFERENCES:

1. Interconnecting Smart Objects with IP: The Next Internet, Jean-Philippe Vasseur, Adam Dunkels, Morgan Kuffmann
2. The Internet of Things: From RFID to the Next-Generation Pervasive Networked Lu Yan, Yan Zhang, Laurence T. Yang, Huansheng Ning
3. Internet of Things (A Hands-on-Approach) , Vijay Madisetti , Arshdeep Bahga
4. Designing the Internet of Things , Adrian McEwen (Author), Hakim Cassimally
5. Asoke K Talukder and Roopa R Yavagal, "Mobile Computing," Tata McGraw Hill, 2010.
6. Computer Networks; By: Tanenbaum, Andrew S; Pearson Education Pte. Ltd., Delhi, 4th Edition
7. Data and Computer Communications; By: Stallings, William; Pearson Education Pte. Ltd., Delhi, 6th Edition
8. F. Adelstein and S.K.S. Gupta, "Fundamentals of Mobile and Pervasive Computing," McGraw Hill, 2009.
9. Cloud Computing Bible, Barrie Sosinsky, Wiley-India, 2010
10. Cloud Security: A Comprehensive Guide to Secure Cloud Computing, Ronald L. Krutz, Russell Dean Vines, Wiley-India, 2010

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6616 Title: **INTERNET OF THINGS (IoT)** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 **The IoT Networking Core :** Technologies involved in IoT Development:	10	25

Internet/Web and Networking Basics OSI Model, Data transfer referred with OSI Model, IP Addressing, Point to Point Data transfer, Point to Multi Point Data transfer & Network Topologies, Sub-netting, Network Topologies referred with Web, Introduction to Web Servers, Introduction to Cloud Computing **IoT Platform overview** Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards. Network Fundamentals: Overview and working principle of Wired Networking equipment's – Router, Switches, Overview and working principle of Wireless Networking equipment's – Access Points, Hubs etc. Linux Network configuration Concepts: Networking configurations in Linux Accessing Hardware & Device Files interactions.		
Module 2 **IoT Architecture:** History of IoT, M2M – Machine to Machine, Web of Things, IoT protocols **Applications:** Remote Monitoring & Sensing, Remote Controlling,Performance Analysis	7	13
FIRST INTERNAL TEST		
The Architecture The Layering concepts , IoT Communication Pattern, IoT protocol Architecture, The 6LoWPAN **Security aspects in IoT**	6	12
Module 3 **IoT Application Development:** **Application Protocols** MQTT, REST/HTTP, CoAP, MySQL **Back-end Application Design** Apache for handling HTTP Requests, PHP & MySQL for data processing, MongoDB Object type Database, HTML, CSS & jQuery for UI Designing, JSON lib for data processing, Security & Privacy during development, Application Development for mobile Platforms: Overview of Android / IOS	10	25

App Development tools		
SECOND INTERNAL TEST		
Module 4 **Case Study & advanced IoT Applications:** IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipments. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino)	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6626

Course Title: MULTIMEDIA COMPRESSION TECHNIQUES

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- Explain the purposes of digital multimedia compression.
- Define different types of compression: lossless and lossy compression.
- Examine the theoretical and practical aspects of the text, image, video and audio compression processes.
- Describe the data redundancies that may be exploited by different types of compression algorithms.
- Address methods in the multimedia compression Huffman coding, DCT-based coding, motion-compensated prediction coding etc.
- Describe the existing multimedia compression standards.

Syllabus:

Special features of Multimedia, Graphics and Image Data Representations, Fundamental Concepts in Video and Digital Audio, Storage requirements for multimedia applications, Need for Compression, Text Compression, Image Compression, Audio Compression and Video Compression.

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the characteristics of different media; understand the representations of different multimedia data; understand different data formats; be able to take into considerations in multimedia system designs.
- Understand the characteristics of human's visual system; understand the characteristics of human's audio system; be able to take into considerations in multimedia techniques design and implementation.
- Understand different compression principles; understand different compression techniques; understand different multimedia compression standards; be able to design and develop multimedia systems according to the requirements of multimedia applications.

TEXT BOOKS:

1. Khalid Sayood: Introduction to Data Compression, Morgan Kauffman Harcourt India, 3rd Edition, 2010

2. David Salomon: Data Compression – The Complete Reference, Springer Verlag New York Inc., 4th Edition, 2006.

REFERENCES:

1. Yun Q. Shi, Huifang Sun: Image and Video Compression for Multimedia Engineering - Fundamentals, Algorithms & Standards, CRC press, 2003.
2. Peter Symes: Digital Video Compression, McGraw Hill Pub., 2004.
3. Mark Nelson: Data compression, BPB Publishers, New Delhi, 2008
4. Mark S. Drew, Ze-Nian Li: Fundamentals of Multimedia, PHI, 1st Edition, 2009.
5. Watkinson, J: Compression in Video and Audio, Focal press, London.1995.
6. Jan Vozer: Video Compression for Multimedia, AP Profes, NewYork, 1995
7. Gonzalez and Woods, Digital Image Processing, 3rd Ed, PHI

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6626 Title: **MULTIMEDIA COMPRESSION TECHNIQUES** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 - Introduction Special features of Multimedia – Graphics and Image Data Representations – Fundamental Concepts in Video and Digital Audio – Storage requirements for multimedia applications -Need for Compression - Taxonomy of compression techniques – Overview of source coding **Text Compression** Compaction techniques – Huffman coding – Adaptive Huffman Coding – Arithmetic coding – Shannon-Fano coding – Dictionary techniques – LZW family algorithms.	10	25

Module 2 - IMAGE COMPRESSION Transform Coding – Discrete Cosine Transform(DCT), Quantization and Coding of Transform Coefficients. JPEG Standard – Sub-band coding algorithms:	7	13
FIRST INTERNAL TEST		
Design of Filter banks – Wavelet based compression: Implementation using filters – EZW, SPIHT coders – JPEG 2000 standard.	6	12
Module 3 - AUDIO COMPRESSION Audio compression techniques - μ- Law and A- Law companding. Frequency domain and filtering – Basic sub-band coding – Application to speech coding – G.722 – Application to audio coding – MPEG audio. Speech compression techniques – LPC and CELP.	10	25
SECOND INTERNAL TEST		
Module 4 - VIDEO COMPRESSION Video compression techniques and standards – MPEG Video Coding I: MPEG – 1 and 2 – MPEG Video Coding II: MPEG – 4 and 7 – Motion estimation and compensation techniques – H.261 Standard – DVI technology – Packet Video. Multimedia Delivery-Multiplexing, Packetization, Time stamping, Synchronization and playback.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6636

Course Title: INFORMATION SECURITY

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

The main goal of this course is to provide the students with the background, foundation and basic approaches in information security. Develop basic understanding of cryptography, how it has evolved, and some key encryption techniques used today. Develop an understanding of security policies as well as protocols to implement such policies in the form of message exchanges. This knowledge will serve as basis for further deeper study into selected areas of the field, or as an important component in further studies

Syllabus:

Introduction to Cryptography, OSI Security Architecture, Modern Cryptography, Public key Cryptography, Introduction to Hash Algorithm, Digital Signature, PKI.

Access Control, Intrusion Detection and Prevention, Firewalls, Malicious Soft wares, Cyber Law and Forensics, Introduction to Network Concepts, Network layer Security, Transport Layer Security, Key management, Application Layer Security, Authentication Applications, Introduction to embedded security, Security Features, Important Rules in Protocol Design, Miniaturization of security, Wireless Security

Course Outcome:

At the end of this course the students will have a comprehensive overview of information security and develop an understanding as to why security and its management are important for any modern organization and how an information security management system should be planned, documented, implemented and improved.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice- William Stallings
2. Practical Embedded Security: Building Secure Resource Constrained Systems - Timothy Stapko, Publisher Newnes.

REFERENCE BOOKS:

1. Cryptography: Theory and Practice – 3rd Ed. SD Stinson, CRC Press.
2. Information Security for Technical Staff-SEI.

3. Guide to firewalls & network security: with intrusion detection & VPNs- HOLDEN, GREG.
4. CISSP: Certified Information Systems Security Professional Study Guide- Stewart, James Michael Et Al.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6636 Title: **INFORMATION SECURITY** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 - Cryptography Introduction to Cryptography: OSI Security Architecture - Security Services, Security Attacks, Security Mechanism. Introduction to Classical Cryptography. Modern Cryptography: Secret key Cryptography - DES, AES. Public key Cryptography - Diffie-Hellman, RSA, ECC. Introduction to Hash Algorithm, Introduction to Digital Signature, Introduction to PKI.	10	25
Module 2 – System Security Introduction - Access Control, Intrusion Detection and Prevention. Firewalls: Firewall Design Principles - Firewall Characteristics, Types of Firewalls. Trusted System.	5	13
FIRST INTERNAL TEST		
Malicious Soft wares: Virus, Trojan Horse, Ad ware/ Spy ware, Worms, Logic Bomb. Cyber Law and Forensics - IT ACT 2000, Cyber Forensics.	5	12
Module 3 - Network Security Introduction to Network Concepts, OSI Layers and Protocols, Network Devices, Network layer Security (IPSec) - IP Security Overview, IPSec	14	25

Architecture, Authentication header, Encapsulating security Payload, Combining Security Associations, Key management. Transport Layer Security - SSL/TLS, SET. Application Layer Security - Authentication Applications, Kerberos, X. 509 Authentication Services. E-mail Security – PGP, S/MIME.		
SECOND INTERNAL TEST		
Module 4 – Embedded Security Introduction, Types of Security Features – Physical, Cryptographic, Platform. Kinds of Devices – CDC, CLDC. Embedded Security Design, Keep It Simple and Stupid Principle, Modularity Is Key, Important Rules in Protocol Design, Miniaturization of security, Wireless Security, Security in WSN.	8	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6646

Course Title: ASIC & SOC

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- To understand ASIC Design flow, standard cell design, synthesis and timing
- To understand the design of Logic cell and IO cell.
- Detailed ASIC Backend design flow and automated design flows for complete ASIC Design.
- Fundamentals of the IP Design and SoC Design.
- To understand SoC Verification flow and complexity in SoC verification.

Syllabus:

Types of ASICs, ASIC Library design, ASIC Construction, System on Chip Design Process, System level design issues- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues; Verification Strategy, On-Chip Buses and Interfaces SoC Verification.

Course Outcome:

After successful completion of the course, students should be able to get:

- Detailed knowledge of ASIC and SoC Design flow.
- Detailed understanding of System on Chip Design process.
- Detailed understanding of complexity in verification and to build SoC Verification environment.

TEXT BOOKS:

1. “SoC Verification-Methodology and Techniques”, Prakash Rashinkar, Peter Paterson and Leena Singh. Kluwer Academic Publishers, 2001.
2. “Reuse Methodology manual for System-On-A-Chip Designs”, Michael Keating, Pierre Bricaud, Kluwer Academic Publishers, second edition, 2001

REFERENCES:

1. Smith, "Application Specific Integrated Circuits", Addison-Wesley,2006

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6646 Title: **ASIC & SOC** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 **Types of ASICs** – Design flow – Economics of ASICs – ASIC cell libraries – CMOS logic cell data path logic cells – I/O cells – cell compilers.	10	25
Module 2 **ASIC Library design:** Transistors as resistors – parasitic capacitance – logical effort programmable ASIC design software: Design system – logic synthesis – half gate ASIC,	7	13
FIRST INTERNAL TEST		
ASIC Construction – Floor planning & placement – Routing	6	12
Module 3 **System on Chip Design Process:** A canonical SoC design, SoC Design Flow – Waterfall vs Spiral, Top-Down versus Bottom-Up. Specification requirements, Types of Specifications, System Design Process, System level design issues- Soft IP vs. Hard IP, Design for Timing Closure- Logic Design Issues, Physical Design Issues; Verification Strategy, On-Chip Buses and Interfaces; Low Power, Manufacturing Test Strategies. MPSoCs. Techniques for designing MPSoCs	10	25
SECOND INTERNAL TEST		
Module 4 **SoC Verification**: Verification technology options, Verification methodology, Verification languages, Verification approaches, and Verification plans. System level verification, Block level verification, Hardware/software co-verification, and Static net list verification.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6656

Course Title: HIGH SPEED DIGITAL DESIGN

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- Teach high-speed design techniques for digital circuits.
- Explain high-speed properties of logic gates.
- To understand power distribution, cross talk and intersymbol interference in electronic systems.
- To understand how the physical layout of signal and return paths affect transmission line characteristics including characteristic impedance, propagation skew, and cross talk.
- To understand timing fundamentals in high speed digital circuits.

Syllabus:

Introduction to high speed digital design, Speed and power -Modeling of wires, Power distribution and noise, Power supply network - local power regulation - IR drops - area bonding, Signaling convention and circuits, Signaling modes for transmission lines -signaling over lumped transmission media, Timing convention and synchronisation, PLL and DLL based clock aligners

Course Outcome:

After successful completion of the course, students should be able to:

- Get a sound understanding of high speed design techniques for digital circuits.
- Recognize good and bad design practices.
- Understand the use of transmission line techniques at the PCB and system levels.
- Understand the importance of clock generation / distribution quality and timing issues in high speed digital circuits.

TEXT BOOKS:

1. Howard Johnson and Martin Graham, "High Speed Digital Design: A Handbook of Black Magic by",3rd Edition, (Prentice Hall Modern Semiconductor Design Series' Sub Series: PH Signal Integrity Library), 2006
2. Stephen H. Hall, Garrett W. Hall, and James A. McCall " High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices by ", Wiley , 2007

REFERENCES:

1. Kerry Bernstein, K.M. Carrig, Christopher M. Durham, and Patrick R. Hansen "High Speed CMOS Design Styles", Springer Wiley 2006
2. Ramesh Harjani "Design of High-Speed Communication Circuits (Selected Topics in Electronics and Systems)" World Scientific Publishing Company 2006

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6656 Title: **HIGH SPEED DIGITAL DESIGN**
(L-T-P): 3-0-0 Credits: 3

Modules	Hours	% marks in ESE
Module 1 **Introduction to high speed digital design.** Frequency, time and distance - Capacitance and inductance effects - High seed properties of logic gates - Speed and power -Modeling of wires -Geometry and electrical properties of wires - Electrical models of wires - transmission lines - lossless LC transmission lines - lossy LRC transmission lines - special transmission lines	10	25
Module 2 **Power distribution and noise** Power supply network - local power regulation - IR drops - area bonding - onchip bypass capacitors - symbiotic bypass capacitors - power supply isolation	7	13
FIRST INTERNAL TEST		
Noise sources in digital system - power supply noise - cross talk - intersymbol interference	6	12
Module 3 **Signaling convention and circuits**	10	25

Signaling modes for transmission lines -signaling over lumped transmission media - signaling over RC interconnect - driving lossy LC lines - simultaneous bi-directional signaling - terminations - transmitter and receiver circuits		
SECOND INTERNAL TEST		
Module 4 **Timing convention and synchronisation** Timing fundamentals - timing properties of clocked storage elements - signals and events -open loop timing level sensitive clocking - pipeline timing - closed loop timing - clock distribution - synchronization failure and metastability - PLL and DLL based clock aligners.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6666

Course Title: EMBEDDED APPLICATIONS IN POWER CONVERSION

Credits: 3-0-0: 3 **Year : 2015**

Pre-requisites: Nil

Objective:

To give the student a foundation in

- power converter design considerations
- design of controllers for power converters
- design considerations for UPS
- design considerations for AC and DC drives

Syllabus:

Power Converters, Practical Converter design considerations, Magnetic components, Design of controllers for Power converters, Interfacing of controller output to power module, Design of UPS, DC Motor Drives, AC Motor Drives

Course Outcome:

After successful completion of the course, the student will have demonstrated an ability to understand the fundamental concepts of power converter design; apply the design consideration for selection of magnetic components, switching components like MOSFET, IGBT etc, controllers and gate drives; apply the basic equations and design considerations for the design of applications like UPS, AC/DC drives, chargers etc.

TEXT BOOKS

1. Power Electronics; By: Mohan, Underland, Robbins; John Wiley & Sons
2. Simplified design of Switching Power supplies; By: John D Lenk; EDN series for designers.

REFERENCES

1. Design of magnetic components for switched mode power converters; By L Umanad, S.R Bhat; Wiely Eastern ltd.
2. MOSFET& IGBT Designers manual, International Rectifier
3. UPS design guide, International Rectifier

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6666 Title: **EMBEDDED APPLICATIONS IN POWER CONVERSION** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Power Converters: Power converter system design. Isolated and Non-isolated dc-dc converters. Inverters with square and sinusoidal output. PWM switching – unipolar and bipolar, sine PWM Practical Converter design considerations: Power semiconductor devices – Power Diodes, BJT, MOSFET, IGBT. MOSFET & IGBT – Ratings, SOA, Switching characteristics, Gate Charge, Paralleling devices. Dos and Don'ts of using Power MOSFETs, Gate drive characteristics & requirements of power MOSFETs and IGBT modules. Design of turn on and turn off snubbers. Magnetic components: Design of high frequency transformer, design of Inductors, design of CTs.	10	25
Module 2 Design of controllers for Power converters: Micro controllers and DSP based controllers for power conversion. Peripheral interfacing - ADC, Keyboard, LCD display, PWM generation.	7	13
FIRST INTERNAL TEST		
Design of PWM bridge controller based on low end and high-end controllers. Interfacing of controller output to power module. Designs based on dedicated gate driver ICs. Design of isolated gate drives.	6	12
Module 3 Design of UPS: Online, off line UPS. Operation & design criteria of AC switch, Operation & design criteria of battery charger, operation & design criteria of inverter, active PFC circuits. Thermal design of power converters.	10	25
SECOND INTERNAL TEST		
Module 4	9	25

DC Motor Drives: Design of adjustable speed DC motor drives, speed control of a separately excited motor, design of closed loop control, design chopper controlled DC motor drive, design of four quadrant chopper. AC Motor Drives: Design of 3 phase PWM VSI inverter, design of v/f control for induction Motor, design of open loop and closed loop control. Vector control of AC motors, space vectors, vector control strategy for induction motor.		
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6676

Course Title: ADVANCED NETWORKING TECHNOLOGIES

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- Build an understanding of the concepts of computer networking.
- Familiarize the student with the basic taxonomy and terminology of the computer networking area.
- Allow the student to gain expertise in some specific areas of networking such as the design and maintenance of individual networks.

Syllabus:

Host Configuration, Connectivity, Testing Path Characteristics, IP next generation – Addressing, Configuration, Ubiquitous Computing – VPN, Understanding Storage Networking, WDM – WDM Network Design – Control and Management – IP Over WDM – Photonic Packet Switching, Monitoring and Control – SNMP, V2, V3, RMON, RMON2.

Course Outcome:

After completing this course the student must demonstrate the knowledge and ability to:

- Independently understand basic and advanced computer network technology.
- Understand and explain Data Communications System and its components.
- Identify the different types of network topologies and protocols.
- Enumerate the layers of the OSI model and TCP/IP.
- Identify the different types of network devices and their functions within a network
- Understand and building the skills of sub-netting and routing mechanisms.
- Familiarity with the protocols of computer networks, and how they can be used to assist in network design and implementation.

REFERENCES:

1. John D. Sloan, “Network Troubleshooting”, Aug’2001 – O’Reilly.
2. Radic Perlman, “Interconnections: Bridges, Routers, Switches and Internetworking Protocols”, Second Edition, Addison Wesley professional, 1999.
3. Andrew S. Tanenbaum, “Modern operating system”, Pearson Education
4. Silvano gai, “Internetworking IPV6 with CISCO Routers”, McGraw– Hill computer communication series.
5. Tom Clark,” Designing Storage Area Network: A practical reference for implementing fiber channel and IP SAN’s”, Second Edition, Addison Wesley professional, 2003.
6. Richard M Barker Paul Massiglia – John Wiley & Sons Inc., “Storage Area Network Essentials: A complete guide to understanding and implementing SANS“, 2001.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6676 Title: **ADVANCED NETWORKING TECHNOLOGIES** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module I Troubleshooting and Management – Host Configuration, Connectivity, Testing Path Characteristics, Packet Capture, Device Discovery and Mapping – Troubleshooting Strategies – Components – Bridges, Routers and Switches – Network OS – Novel Netware, Linux.	10	25
Module II IP next generation – Addressing, Configuration, Security, QOS - VOIP- Issues in VOIP – Distributed Computing and Embedded System – Ubiquitous Computing - VPN	7	13
FIRST INTERNAL TEST		
Understanding Storage Networking – Storage Networking Architecture – The Storage in Storage Networking, The Network in Storage Networking, Basic Software for Storage Networking – SAN Implementation Strategies.	6	12
Module 3 WDM – WDM Network Design – Control and Management – IP Over WDM – Photonic Packet Switching.	10	25
SECOND INTERNAL TEST		
Module 4 Monitoring and Control – SNMP, V2, V3, RMON, RMON2.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6686

Course Title: ELECTRONIC PACKAGING

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- The objective of this course is to sensitize the students to the all-important multidisciplinary area of electronics systems packaging.
- The course will discuss all the important facets of packaging at three major levels, namely, chip level, board level and system level.
- The entire spectrum of microelectronic systems packaging from design to fabrication; assembly and test will be covered. Current trends in packaging of electronic systems will be covered.

Syllabus:

Overview of electronic systems packaging, Definition of PWB, Wafer fabrication, inspection and testing, Wafer packaging, Commonly used packages and advanced packages, Electrical Issues, Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights, Design Flow considerations, Photo plotting and mask generation, Process flow-chart

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the basics and advanced concepts of electronic packaging schemes
- Understand the current trends and special topics of packaging

TEXT BOOKS:

1. Rao R. Tummala, Fundamentals of Microsystems Packaging, McGraw Hill, NY, 2001.

REFERENCES:

1. William D.Brown,Advanced Electronic Packaging, IEEE Press, 1999.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks

Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC6686 Title: **ELECTRONIC PACKAGING** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1: Overview of electronic systems packaging, Definition of a system and history of semiconductors, Products and levels of packaging, Packaging aspects of handheld products; Case studies in applications, Definition of PWB. Video on "Sand-to-Silicon", Wafer fabrication, inspection and testing, Wafer packaging; Packaging evolution; Chip connection choices, Wire bonding, TAB and flipchip-1,Wire bonding, TAB and flipchip-2.	10	25
Module 2: Necessary of packaging. Types , Single chip packages or modules (SCM), Commonly used packages and advanced packages; Materials in packages, Thermal mismatch in packages; Current trends in packaging, Multichip modules (MCM)-types; System-inpackage (SIP); Packaging roadmaps; Hybrid circuits;	7	13
FIRST INTERNAL TEST		
Electrical Issues – I; Resistive Parasitic , Electrical Issues – II; Capacitive and Inductive Parasitic, Electrical Issues – III; Layout guidelines and the Reflection problem, Electrical Issues – IV; Interconnection.	6	12
Module 3 Benefits from CAD to packages; Introduction to DFM, DFR & DFT 20. Components of a CAD package and its highlights, Design Flow considerations; Beginning a circuit design with schematic work and component layout , Demo and examples of layout and routing; Technology file generation from CAD; DFM check list and design rules; Design for Reliability. Review of CAD output files for PCB fabrication; Photo plotting and mask generation, Process flow-chart; Vias; PWB substrates, Substrates continued; Video highlights; Surface preparation, Photoresist and application methods; UV exposure and developing; Printing technologies for PWBs, PWB	10	25

etching; Resist stripping; Screen-printing technology, Through-hole manufacture process steps; Panel and pattern plating methods. Video highlights on manufacturing; Solder mask for PWBs; Multilayer PWBs; Introduction to microvias, Microvia technology and Sequential build-up technology process flow for high-density interconnects, Conventional Vs HDI technologies; Flexible circuits; Tutorial session.		
SECOND INTERNAL TEST		
Module 4 SMD benefits; Design issues; Introduction to soldering, Reflow and Wave Soldering methods to attach SMDs, Solders; Wetting of solders; Flux and its properties; Defects in wave solderin, Vapour phase soldering, BGA soldering and Desoldering/ Repair; SMT failures, SMT failure library and Tin Whiskers, Tin-lead and lead-free solders; Phase diagrams; Thermal profiles for reflow soldering; Lead-free alloys, Lead-free solder considerations; Green electronics; RoHS compliance and e-waste recycling issues. Thermal Design considerations in systems packaging, Introduction to embedded passives; Need for embedded passives; Design Library; Embedded resistor processes Embedded capacitors; Processes for embedding capacitors; Case study.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC6662

Course Title: MINI PROJECT

Credits: 0-0-4: 2 Year : 2015

Pre-requisites: Nil

Objective:

- *To apply the embedded concepts introduced in the courses to a moderately complex embedded system.*

Syllabus:

The students can select hardware, software or system level mini projects. The mini project can be implemented using **Microcontroller or DSP or FPGA or RTOS** tools which they have studied. A complete product or project can be selected. The project can be done individually or as a group of two students.

Course Outcome:

After successful completion of the mini project, students should get the necessary confidence to take up bigger embedded challenges

REFERENCES:

Manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Internal continuous assessment is in the form of evaluation, demonstration, presentation etc. The assessment details are to be announced to the students, right at the beginning of the semester by the teacher.

Attendance & Regularity	20 Marks
Evaluation I	30 Marks
Evaluation II	30 Marks
Assessment by Guide	20 Marks
Total	**100 Marks**

Course No: 09EC6672

Course Title: DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS - LABORATORY

Credits: 0-0-2: 1 Year : 2015

Pre-requisites: Nil

Objective:

To make the students practically implement various DSP algorithms.

Syllabus:

DSP basic experiments using ARM Cortex M3/M4, implementation of Digital Signal Processing Algorithms such as DFT, FFT etc using MATLAB, Real-Time Implementation of DSP algorithms such as DFT, FFT, DTMF etc on a Microcontroller or DSP Processor, Cooley - Tukey FFT Algorithm implementation using FPGA.

Course Outcome:

After successful completion of the course, students should be able to:

- Implement FFT, Filter, DTMF algorithms on a Microcontroller or DSP.
- Get confidence to Implement any DSP algorithm on any processor

REFERENCES:

1. Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform, 1st Edition; by: Naim Dahnoun
2. DSP Applications using 'C' and the TMS320C6X DSK, 1st Edition; by: Rulph Chassaing
3. Digital Signal Processing with Field Programmable Gate Arrays: 2nd Edition, by: U. Meyer – Base, Springer
4. Digital Signal Processing: A System Design Approach, 1st Edition; by: David J Defatta J, Lucas Joseph G & Hodkiss William S; John Wiley
5. Real - Time Digital Signal Processing: Implementations, Applications, and Experiments with the TMS320C55X, Kuo, Sen M, Lee, Bob H, John Wiley & Sons
6. Digital Signal Processing – Architecture, Programming and Applications, by: B. Venkataramani & M.Bhaskar; Tata McGraw Hill
7. Digital Signal Processing - A Student Guide, 1st Edition; by: T.J. Terrel and Lik-Kwan Shark; Macmillan Press; Ltd.

In addition, National/ International journals in the field, manufacturers Device data sheets and application notes and research papers in journals are to be referred to get practical and application oriented information.

Internal Continuous Assessment: 100 marks

Mid Term Internal Test	40 Marks
Laboratory Experiments & Viva Voce	10 Marks
Final Internal Test	50 Marks
Total	**100 Marks**

COURSE PLAN:

Course No: 09EC6672 Title: **DESIGN OF DIGITAL SIGNAL PROCESSING SYSTEMS - LABORATORY**
(L-T-P): 0-0-2 Credits: 1

Modules	Hours	% marks in ESE
Module 1 **Module 1 - DSP Fundamentals using ARM Cortex M3/M4:** Experiment 1: Write a program to implement convolution of x(n) with h(n) using linear convolution and verify the result y(n) as below. x(n) = [1,1,1,1,0.5,0.5,0.5,0.5] , h(n) = [0.3,0.25,0.2,0.15,0.1,0.05] and y(n) == [0.3, 0.55,0.75,0.9,0.85,0.775,0.675,0.6,0.4.0.25,0.15,0.075,0.025] Experiment 2: Write a program for circular convolution of the following inputs x(n) and h(n) and Verify the output y(n) as given below. x(n) = [1,1,1,2,1,1] , h(n) = [1,1,2,1] and y(n) = [6,5,5,6,6,7] Experiment 3: Implement an 8-point DFT for the inputs x(n) and verify the result as X(K). Where, x(n) = [1,1,1,1,1,1,0,0] and X(K) = [6,-0.707-j1.707,1-j,0.707+j0.293,0,0.707-j0.293,1+j,-0.707+j1.707]. Experiment 4: Find IDFT of the sequence X(K) = [11110000]. Verify that x (n) = [0.5,0.125+j0.30175, 0,0.125+j0.05175, 0,0.125-j0.05175, 0,0.125-j0.30175] Experiment 5: Generate the following waveforms using the DAC of ARM Cortex M3/M4and verify the outputs for different frequencies (1KHz, 2KHz etc.) a. Sine wave b. Square wave	6	25

Experiment 6: Tone Generation using the DAC of ARM Cortex M3/M4. 1. Generate a simple tone of a fixed frequency (1 KHz). 2. Generate multiple tones using DAC at frequencies starting from 300Hz to 3 KHz with an increment of 100Hz each tone for duration of 1second using timer interrupt.		
Module 2 **Module 2 - Digital Signal Processing Algorithms:** Experiment 1: Design an FIR Low pass Filter with following specification. fp = 1500Hz, fs = 2000Hz, Pass band attenuation = 0.01dB, Stop band attenuation = 40dB and Fs = 8000 Hz using Kaiser window. Experiment 2: Write programs for DFT, FFT using Matlab	8	25
FIRST INTERNAL TEST		
Module 3 - Digital Signal Processing Application: Experiment 1: Real-time Implementation of FIR filters 1. Generate the filter coefficients using Kaiser Window for a low pass FIR filter for the specification as given in experiment 1 of module 2. 2. Apply an input signal through ADC and implement the filter on ARM Cortex M3/M4. Vary the input signal frequency and observe the output on an Oscilloscope. 3. Repeat the filter for Band pass and High pass. 4. Repeat the same with hamming window. Experiment 2: Fourier Transform Perform FFT analysis for the signal input through ADC and display the input signal as well as the FFT output on PC using Probe point facility. Perform FFT operation for 16, 32 and 64-point FFT. Compute the power spectrum X(K) * X(K) = $\|X(K)\|^2$ = $Xreal^2$ + $Ximag^2$ and plot the same in PC. Experiment 3: DTMF Tone Generation and Detection and its implementation. Generate DTMF Tones. Detect the DTMF tone input trough the ADC. Implement the program with Geortzel algorithm. Experiment 4: Implementation of Speech processing applications	10	25
Module 4 **Module 4 - Current trends in Digital Signal Processor (any two):**	4	25

Implementation of Serial/Parallel Convolver using FPGAs Implementation of a length four FIR filter using VHDL Designing a four-tap Direct FIR filter using VHDL Cooley - Tukey FFT Algorithm implementation using FPGA		
SECOND INTERNAL TEST		
Total Hours	**28**	

Software used: Code Composer Studio, Matlab, Xilinx Foundation series

Platforms used: PC, ARM Cortex M3/M4 Starter Kits, Xilinx/ Altera FPGA Kits

THIRD SEMESTER

ES 15 301 - ELECTIVE IV
&
ES 15 302 - ELECTIVE V

Course No: 09EC7617

Course Title: WIRELESS TECHNOLOGIES

Credits: 3-0-0: 3 **Year : 2015**

Pre-requisites: Nil

Objective:

- This subject is framed to set the required background in wireless communication. Being the backbone for all the IT based developments; Wireless Technology has seen tremendous growth in the past decade. There are new techniques and protocols emerging from time-to-time to cater the requirements of this rapidly growing area.
- The subject will cover from rf fundamentals to the topics like celluar, WiFi, WPN and WSN technologies.
- The treatment would look at current and upcoming wireless communications technologies for various wireless accesses.

Syllabus:

Radio Frequency (RF) Fundamentals, Spread Spectrum Concepts, RF Antenna Concepts, Cellular Standards, WLAN, Wi-Fi Organizations and Standards, Wi-Fi Hardware & Software, WSN & WPN, IEEE 802.15 standards, ZigBee, Sub1GHz, Sensor Networks, Interfacing problems and co-existence strategies in Sensor Networks, Routing protocols in Wireless Sensor Networks.

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the different wireless technologies available today.
- Understand the basics of embedded wireless application development.

TEXT BOOKS:

1. Wireless Communications – Principles and Practice; by Theodore S Rappaport, Pearson Education Pte. Ltd., Delhi
2. Wireless Communications and Networking; By: Stallings, William; Pearson Education Pte. Ltd., Delhi

REFERENCES:

1. Bluetooth Revealed; By: Miller, Brent A, Bisdikian, Chatschik; Addison Wesley Longman Pte Ltd., Delhi
2. Wilson , "Sensor Technology hand book," Elsevier publications 2005.
3. Andrea Goldsmith, "Wireless Communications," Cambridge University Press, 2005
4. Mobile and Personal Communications Services and Systems; 1st Edition; By: Raj Pandya; PHI, New Delhi
5. Fundamentals of Wireless Communication by Tse David and Viswanath Pramod, Cambridge University press, Cambridge
6. Mobile Communications; By: Schiller, Jochen H; Addison Wesley Longman Pte Ltd., Delhi
7. 3G Networks: Architecture, protocols and procedures based on 3GPP specifications for UMTS WCDMA networks, By Kasera, Sumit, Narang, and Nishit, TATA MGH, New Delhi
8. Wireless Sensor Networks: information processing by approach, ZHAO, FENG, GUIBAS and LEONIDAS J, ELSEVIER, New Delhi
9. Holger Karl and Andreas Wiilig, "Protocols and Architectures for Wireless Sensor Networks" John Wiley & Sons Limited 2008.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7617 Title: **WIRELESS TECHNOLOGIES** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 - RF Basics: **Radio Frequency (RF) Fundamentals:** Introduction to RF & Wireless Communications Systems, RF and Microwave Spectral Analysis, Communication Standards, Understanding RF & Microwave Specifications. Spectrum Analysis of RF Environment, Protocol Analysis of RF Environment, Units of RF measurements, Factors affecting network range and speed, Environment, Line-of-sight, Interference, Defining differences	10	25

between physical layers- OFDM, HR/DSSS,MIMO **Spread Spectrum Concepts:** OFDM & HR/DSSS channels, Co-location of HR/DSSS and OFDM systems, Adjacent-channel and co-channel interference, WLAN / WPAN co-existence, CSMA/CA operations **RF Antenna Concepts:** Passive gain, Beam widths, Simple diversity, Polarization, Antenna Mounting, Wireless Antennas and Accessories, RF cables, RF connectors, Lightning arrestors and grounding rods		
Module 2 – Cellular Standards Cellular carriers and Frequencies, Channel allocation, Cell coverage, Cell Splitting, Microcells, Picocells, Handoff	7	13
FIRST INTERNAL TEST		
1st, 2nd, 3rd and 4th Generation Cellular Systems (GSM, CDMA,IS-95, GPRS, EDGE,UMTS, EVDO, CDMA2000), Mobile IP, WCDMA	6	12
Module 3 – WLAN **Wi-Fi Organizations and Standards:** Regulatory Bodies, IEEE, Wi-Fi Alliance, WLAN Connectivity, WLAN QoS & Power-Save, IEEE 802.11 Standards,802.11-2007,802.11a/b/g, 802.11e/h/I,802.11n **Wi-Fi Hardware & Software:** Access Points, WLAN Routers, WLAN Bridges, WLAN Repeaters, WLAN Controllers/Switches, Direct-connect Aps, Distributed-connect Aps, PoE Infrastructure, Midspan, Endpoint, Client hardware and software, Antenna types and uses Wi-Fi Security concepts, Wi-Fi Applications	10	25
SECOND INTERNAL TEST		
Module 4 **Module 4 – WSN & WPN** Wireless Personal Area Networks, Bluetooth, Bluetooth Standards, BlueTooth Protocol Architecture,UWB, IEEE 802.15 standards, ZigBee, Sub1GHz, Sensor Networks, Interfacing problems and co-existence strategies in Sensor Networks, Routing protocols in Wireless Sensor Networks.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7627

Course Title: AUTOMOTIVE ELECTRONICS

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

To give the Student:-

- A foundation in physical configuration of the automobile
- A foundation in electronic and digital engine control systems
- A foundation in vehicle motion control and diagnostics

Syllabus:

Automotive fundamentals, Characteristics of digital electronic system, Instruments, Control system, Basics of Electronic Engine control, Sensors and actuators, Digital Engine control system, Vehicle motion control, Cruise control system, Antilock braking system, Electronic suspension system

Course Outcome:

Students who successfully complete this course will have demonstrated an ability to understand the working of various subsystems of a modern automobile; compare various control strategies, understand the interfacing requirements for various sensors and actuators; understand the requirements of electronic and digital engine control systems; understand the requirements of motion control and onboard and off board diagnostics system.

TEXT BOOK

1. William B. Ribbens " Understanding Automotive Electronics" 6th Edition, Newnes

REFERENCE

1. Betchtold., " Understanding Automotive Electronics" SAE, 1998

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7627 Title: **AUTOMOTIVE ELECTRONICS** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Automotive fundamentals: Automotive physical configuration, Engine, ignition system, drive train, suspension, brakes, steering system. Systems approach to control and instrumentation: Characteristics of digital electronic system, Instruments, Control system.	10	25
Module 2 Basics of Electronic Engine control: Motivation for electronic engine control, concept of an electronic engine control, definition of engine performance terms, Engine Mapping, control strategy, electronic fuel control system, electronic ignition.	7	13
FIRST INTERNAL TEST		
Sensors and actuators: Air flow rate sensor, engine crank shaft angular position sensor, throttles angle sensor, temperature sensor, oxygen sensor, knock sensor. Automotive engine control actuators.	5	12
Module 3 Digital Engine control system: Digital Engine control features, control modes for fuel control, EGR control, Electronic ignition control, integrated engine control system.	10	25
SECOND INTERNAL TEST		
Module 4 Vehicle motion control: Cruise control system, Antilock braking system, Electronic suspension system, Electronic steering control, automotive instrumentation, on board and off – board diagnostics, occupant protection systems.	10	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7637

Course Title: MIXED SIGNAL SYSTEM DESIGN

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- To introduce the principles of Analog Mixed Signal System Design.
- Design and Analysis of Complex Digital and Analog CMOS Circuits to provide a foundation for more complicated and advanced Designs.
- To introduce the concept of switched capacitor techniques.
- To address practical issues in Analog Mixed Signal System Design

Syllabus:

PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, CMOS Logic implementation basics, TG based implementation of multiplexers, de-multiplexers, encoders, decoders, ALU, Comparator, Parity generator, Timer, PWM,SRAM and DRAM,CAM, Analog Sub circuits, Ideal Operational Amplifier, Inverting and Non-inverting configuration Differential amplifier basics, VCO, PLL, Data Converters, DAC, ADC, Over sampling Data Converters

Course Outcome:

After successful completion of the course, students should be able to:

- Detailed knowledge of static and dynamic behavior of CMOS logic.
- Detailed understanding of CMOS Digital Subsystem Design.
- Timing analysis and synchronization of digital design.
- Basic understanding of Analog circuit building blocks.
- Detailed understanding of Analog Mixed Signal Circuit Design.
- Detailed Understanding of Data Converters.

TEXT BOOKS:

1. CMOS Analog Circuit Design, 2nd edition; by: Allen, Phillip E, Holberg , Douglas R, Oxford University Press, (Indian Edition
2. D A John, Ken Martin, Analog Integrated Circuit Design, 1st Edition, John Wiley

REFERENCES:

1. Ken Martin, Digital Integrated Circuit Design, John Wiley
2. Gray Paul R, Meyer, Robert G, Analysis and Design of Analog Integrated Circuits, 3rd edition, John Wiley & Sons.
3. Sedra & Smith, Microelectronics Circuits, 5th Edition, Oxford University Press, (Indian Edition)
4. Jan M. Rabaey, Anantha Chadrakasan, B. Nikolic ,Digital Integrated Circuits – A Design Perspective 2nd Edition, Prentice Hall of India (Eastern Economy Edition).

5. Sung-Mo Kang**,** Yusuf Leblebici, CMOS Digital Integrated Circuits Analysis & Design,2nd Ed, Tata McGraw Hill

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7637 Title: **MIXED SIGNAL SYSTEM DESIGN** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Introduction PN Junctions, Bipolar Vs Unipolar Devices, MOS Transistor operation, MOS Transistor as a Switch, NMOS ,PMOS and CMOS Switches, CMOS Inverter AC and DC Characteristics, Analog Signal Processing, Example of Analog Mixed Signal Circuit Design	10	25
Module 2 Digital Sub Circuits CMOS Logic implementation basics- Logic gates and Flip flops –Transmission Gates, TG based implementation of multiplexers, de-multiplexers, encoders, decoders.	7	13
FIRST INTERNAL TEST		
Digital Circuits like ALU, Comparator, Parity generator, Timer, PWM,SRAM and DRAM,CAM	6	12
Module 3 Analog Sub circuits Ideal Operational Amplifier, Inverting and Non-inverting configuration Differential amplifier basics, VCO, PLL, Comparator characteristics, two stage open loop comparator ,Switched capacitor fundamentals, Switched capacitor amplifier	10	25
SECOND INTERNAL TEST		

Module 4 **Module 4 Data Converters** **DAC** : Static &Dynamic Charatersitics,1 Bit DAC, String DAC, Fully Decoded DAC,PWM DAC, Current scaling, voltage scaling DACs **ADC** : Static &Dynamic Characteristics, Nyquist Criteria , Sample & Hold Circuit ,Quantization error, Concept of over sampling, Counting ADC, Tracking ADC, Successive approximation ADC, Flash ADC, Dual Slope ADC **Over sampling Data Converters** : Over sampling fundamentals, Delta – Sigma Converter basics, $\Delta \sum$ Modulator	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7647

Course Title: ROBOTICS AND MACHINE VISION

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- To introduce the concepts of Industrial Robots and Machine Vision and Image Processing techniques for industrial applications.

Syllabus:

Classification and Structure of Robotic Systems, Kinematics Analysis and Coordinate Transformations, Machine Vision, Industrial Robots, Image Processing Techniques and Transformations, Basic Machine Vision Processing Operators – Monadic one Point Transformations, Edge Enhancement Techniques and Image Analysis, Thresholding, Pattern Matching and Edge Detection, Back-Propagation Algorithm.

Course Outcome:

After successful completion of the course, students should be able to:

- Get a clear idea of the Image processing and analysis techniques used in Machine Vision for industrial application

TEXT BOOKS:

1. Machine Vision and Digital Image Processing, by Louis J. Galbiati, Jr. Prentice Hall, Englewood Cliffs, New Jersy.`
2. Robotics for Engineers, By, Yoram Koren, McGraw Hill.

REFERENCES:

1. Robotics and Image Processing – an Introduction, by Janakiraman P. A., Tata McGraw Hill, New Delhi
2. Digital Image Processing and Computer Vision by Robert J.Schalkoff, John Wiley & Sons Inc.
3. Industrial Robotics – Technology, Programming and Applications, by Mikell P. Groover, Mitchell Wein, Roger N. Nagel and Nicholas G. Odlrey, McGraw Hill International Edistion.
4. Handbook Of Image Processing Operators by Klette, Reinhard & Zamperoni, Piero; John Wiley & Sons Inc
5. Image Processing, Analysis And Machine Vision by Sonka, Milan Et Al
6. Industrial Robotics by Hodges, Bernard, Jaico Publishing House, Delhi

7. Introductory Computer Visiona dn Image Processing by Adrian Low, McGraw Hill International Editions.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7647 Title: **ROBOTICS AND MACHINE VISION** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 - Industrial Robots: Basic Concepts of Robotics, Classification and Structure of Robotic Systems Kinematics Analysis and Coordinate Transformations, Industrial Applications of Robots, and Programming	10	25
Module 2 - Introduction Machine Vision: Principles of Machine Vision, Vision and factory automation, Human Vision Vs. Machine Vision, Economic Considerations, Machine Vision – System Overview, Image acquisition – Illumination, Image formation and Focusing,	7	13
FIRST INTERNAL TEST		
Image Detection – Introduction, Types of Cameras; Image Processing and Presentation.	6	12
Module 3 - Image Processing Techniques and Transformations: Fundamental Concepts of Image Processing, Pixel, Pixel Location. Gray Scale, Quantizing Error and Measurement Error and Histograms. Basic Machine Vision Processing Operators – Monadic one Point Transformations: Identity operator, Inverse Operator, Threshold operator and other operators viz: Inverted Threshold operator, Binary Threshold operator, Inverted Binary Threshold Operator, Gray Scale Threshold and Inverted Gray Scale Threshold Operators;	10	25

Dyadic Two Point Transformations –Image Addition, Image Subtracting, Image Multiplication; Convolution and Spacial Transformations		
SECOND INTERNAL TEST		
Module 4 **Module 4 - Edge Enhancement Techniques and Image Analysis:** Introduction, Digital Filters – Low pass and High Pass filters; Edge Engancement Operators – Laplacian, Roberts Gradient, Sobel and other Local operators. Image Analysis: Thresholding, Pattern Matching and Edge Detection, Back-Propagation Algorithm.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7657

Course Title: ELECTRONIC INSTRUMENTATION DESIGN

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

The objective of this subject is to introduce the students to the design concepts of Electronic Instrumentation techniques such as Instrumentation amplifier and Error Budgeting, Smart Sensors etc.

Syllabus:

Architecture of Instrumentation scheme, Principle and design of various active and passive transducers, Electrical I/O characteristics of sensors/transducers, Amplification, attenuation, isolation, multiplexing, filtering, linearization, compensation, simultaneous sampling & transducer excitation, Analog Signal Acquisition, Conditioning and Processing, Sampled Data, Conversion System Design with Computer, Introduction to smart sensors, Voltage to Frequency Converters and Frequency to Code converters, Data Acquisition methods for multi Channel sensor systems

Course Outcome:

After successful completion of the course, students should be able to:

- Design the necessary signal conditioning and acquisition circuits required for various embedded applications.

TEXT BOOKS:

1. Measurement and Instrumentation Principles, by: Alan S. Morris, Butterworth-Heinemann
2. Advanced Instrumentation and Computer I/O Design, by: Patrick H. Garrett, IEEE Press.

REFERENCES:

1. Data Acquisition and Signal Processing for Smart Sensors, by: Nikolay V. Kirianaki et al., John Wiley & Sons
2. Microsensors MEMS and Smart Devices, by: Julian W. Gardner, Vijay K. Varadan, et al., John Wiley & Sons
3. Industrial Instrumentation Principles and Design, 1st edition; by:Tattamangalam. R.Padmanabhan, Springer Verlag.
4. Measurement Systems Application and Design, by: Ernest O. Doebelin, McGraw-Hill Science/Engineering/Math
5. Handbook of Transducers, 1st edition; by: Harry N.Norton, Prentice Hall.
6. Advances in Distributed Sensor Technology; by: S.S.Iyengar, L.Prasad, Hla Min; Prentice Hall PTR

7. Standard Recommended Practises for Instrumentation & Control, Vol 1-3,11th edition; Instrument Society of America.
8. Microsensors: Principles and Applications; by: Gardner, J W, Wiley (1994)
9. Measurement Systems, Application and Design, 4th edition; by: Ernest O.Doebelin, McGraw- Hill.
10. Practical Design Techniques For Sensor Signal Conditioning; Seminar Materials@ http://www.analog.com
11. Data Acquisition Fundamentals; Application Note AN007 @ http://www.ni.com
12. Measurement Systems And Sensors (Hardcover), By: Waldemar Nawrocki , Artech House Publishers
13. Microtransducer CAD: Physical and Computational Aspects (Computational Microelectronics) (Hardcover), by: Arokia Nathan (Author), Henry Baltes (Author), Springer

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :

Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7657 Title: **ELECTRONIC INSTRUMENTATION DESIGN** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1 Architecture of Instrumentation scheme. Static and dynamic characteristics, errors, standards and calibration. Principle and design of various active and passive transducers. Introduction to semiconductor sensors and its applications. Electrical I/O characteristics of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion. Specifications and selection of sensors/transducers for measurement of temperature, flow, level, pressure, position and motion.	10	25
Module 2 Amplification, attenuation, isolation, multiplexing, filtering, linearization, compensation, simultaneous sampling & transducer excitation. Operational and Instrumentation Amplifiers.	7	13
FIRST INTERNAL TEST		

Instrumentation amplifiers and Error Budgets, Noise in low level Amplification.	6	12
Module 3 Analog Signal Acquisition, Conditioning and Processing, Input grounding, Shielding and Termination Practice. Signal conditioning Error Analysis. DC, Sinusoidal and Harmonic Signal Conditioning, Analog Signal Processing, Devices for Data Conversion – Analog Multiplexers, Sample – Holds, D/A and A/D Sampled Data, Inter sample Error and Interpolation, Aliasing of Signal and Noise, Inter sample and Aperture Error, Signal Recovery and Interpolation Conversion System Design with Computer – Assisted Analysis, System Design Considerations, Computer Assisted Interface Analysis Software	10	25
SECOND INTERNAL TEST		
Module 4 Introduction to smart sensors, Voltage to Frequency Converters and Frequency to Code converters, Data Acquisition methods for multi Channel sensor systems, Smart sensor design, Smart sensor Buses and Interface circuits.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7667

Course Title: ADVANCED DIGITAL COMMUNICATION

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- The course presents the fundamental techniques of generation, transmission, and reception of communication system related signals applicable for a wide range of communication applications.
- System design for optimum performance has been thoroughly covered in this presentation.
- A module on the synchronization techniques has been included.
- Communication system design for communication over fading channels has been covered in detail.

Syllabus:

Digital communication system, Pulse amplitude modulation (binary and M-ary, QAM), Continuous phase modulation (QPSK and variants, MSK, GMSK), Coherent and non-coherent demodulation, Optimum rule for ML and MAP detection Performance, Pulse shape design for channels with ISI, Performance: Symbol by symbol detection and BER, Viterbi algorithm, synchronization techniques, Characteristics of fading channels, Rayleigh and Rician channels, receiver performance-average SNR, outage probability

Course Outcome:

After successful completion of the course, students should be able to:

- Understand the advanced concepts of digital communication .
- Latest trends in digital communication area.

TEXT BOOKS:

1. J. G. Proakis and M. Salehi, Fundamentals of Communication Systems, Pearson Education, 2005.
2. S. Haykins, Communication Systems, 5th ed., John wiley, 2008.

REFERENCES:

1. M. K. Simon, S. M. Hinedi and W. C. Lindsey, Digital Communication Techniques: Signaling and detection, Prentice Hall India, N. Delhi, 1995.
2. W. Tomasi, Advanced Electronic Communication Systems, 4th Ed., Pearson Education, 1998.

3. M. K. Simon and M. S. Alouini, Digital Communication over Fading Channels, 2000.
4. Simon Haykin,Digital Communications , 2006, John Wiley & Sons.
5. B.P. Lathi,Modern Digital and Analog Communication, 3rd Ed., Oxford UniversityPress.
6. Sklar, Digital Communication, 2E, Pearson Education.
7. K.Sam Shanmugham,Digital and Analog Communication Systems, John Wiley &Sons
8. R.E. Ziemer and W.H. Tranter,Principles of Communications, JAICO PublishingHouse.
9. H.Taub and Schilling,Principles of Communication Systems, TMH
10. Pierre Lafrance,John G.Proakis,Digital Communications, McGraw Hill.
11. Couch, Analog and Digital Communication.5th Ed,PHI

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7667 Title: **ADVANCED DIGITAL COMMUNICATION** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1: Digital communication system (description of different modules of the block diagram), Complex baseband representation of signals, Gram-Schmidt orthogonalization procedure. M-ary orthogonal signals, bi-orthogonal signals, simplex signal waveforms. Pulse amplitude modulation (binary and M-ary, QAM), Pulse position modulation (binary and M-ary), Carrier modulation (M-ary ASK, PSK, FSK, DPSK), Continuous phase modulation (QPSK and variants, MSK, GMSK).	10	25
Module 2 Coherent and non-coherent demodulation: Matched filter, Correlator demodulator, square-law, and envelope detection;	7	13
FIRST INTERNAL TEST		
Detector: Optimum rule for ML and MAP detection Performance: Bit-error-	6	12

rate, symbol error rate for coherent and non-coherent schemes.		
Module 3 Pulse shape design for channels with ISI: Nyquist pulse, Partial response signaling (duo binary and modified duo binary pulses), demodulation; Channel with distortion: Design of transmitting and receiving filters for a known channel and for time varying channel (equalization); Performance: Symbol by symbol detection and BER, symbol and sequence detection, Viterbi algorithm.	10	25
SECOND INTERNAL TEST		
Module 4 Different synchronization techniques (Early-Late Gate, MMSE, ML and spectral line methods). Characteristics of fading channels, Rayleigh and Rician channels, receiver performance-average SNR, outage probability, amount of fading and average bit/symbol error rate.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7677

Course Title: VLSI SIGNAL PROCESSING

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- To cover techniques for designing efficient DSP architectures.
- To realize DSP architectures that will process high throughout data end/or require less power and / or less chip area.
- To learn a complete DSP system and fundamentals of pipelining and parallel processing on FIR filters
- To study the concepts of retiming, unfolding, transforms and rank order filters.
- To study different bit level architectures and their complexities
- To realize array signal processing structures like spatial filter

Syllabus:

Graphical representation of DSP algorithms, Dataflow and control flow, Unfolding, Folding, Design of VLSI Architectures for Digital Signal Processing, Speed-Area-Power tradeoff issues related to mixed signal design and SoC, Filter structures, Transform structures, Data Flow and Control flow issues, Modern DSP algorithms, VLSI Architecture development for JPEG2000 video CODEC and performance comparisons

Course Outcome:

After successful completion of the course, students should be able to:

- Understand various signal processing algorithms that can be designed and applied on application specific VLSI architecture
- Have the knowledge on introducing pipelining, parallism, in place memory and high speed multipliers, used to improve the efficiency of DSP processors
- Analyze different number representations, arithmetic based binary representations and complexities involved in it for easier numerical computations on processors.
- Gain minimum knowledge to find solution for any research queries on DSP processors.

TEXT BOOKS:

1. VLSI Signal Processing Systems - Keshab K Parhi, John Wiley and Son's, NY 1999.
2. Architectures for Digital Signal Processing - Peter Prissch, John Wiley and Son's NY 1998.

REFERENCES:

1. Introduction to Data Compression, 2nd Edition - Khalid Sayood, Harcourt India, New Delhi, 2000.

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7677 Title: **VLSI SIGNAL PROCESSING** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1: Graphical representation of DSP algorithms, Dataflow and control flow. Introduction to Pipelining and Parallel Processing, Parallel pipelined design of DSP Algorithms. Retiming: Introduction, Definition and properties, Solving system of inequalities, retiming techniques. Unfolding Introduction, An algorithms for unfolding, Properties of unfolding, Critical path, unfolding and retiming Application of unfolding. Folding: Introduction Folding Transformation, Register Minimization Techniques, Register minimization in folded architectures	10	25
Module 2: Design of VLSI Architectures for Digital Signal Processing: Architectural Design at Register Transfer Level, Design of Data path elements, Control structures	7	13
FIRST INTERNAL TEST		
Testable and self-reconfigurable fault-tolerant structures. Speed-Area-Power tradeoff issues related to mixed signal design and SoC.	6	12
Module 3 Filter structures, Transform structures, Data Flow and Control flow issues. Array processing approaches to DSP solutions. Introduction to spatial filters. Development of VLSI architecture for spatial filter.	10	25

SECOND INTERNAL TEST		
Module 4 Modern DSP algorithms (Audio, Video and Multimedia) and development of new computational and arithmetic building blocks. VLSI Architecture development for JPEG2000 video CODEC and performance comparisons.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7687

Course Title: CLOUD COMPUTING

Credits: 3-0-0: 3 Year : 2015

Pre-requisites: Nil

Objective:

- The objective of this course is to provide students with the comprehensive and in-depth knowledge of Cloud Computing concepts, technologies, architecture and applications by introducing and researching state-of-the-art in Cloud Computing fundamental issues, technologies, applications and implementations.
- Another objective is to expose the students to frontier areas of Cloud Computing and information systems, while providing sufficient foundations to enable further study and research.

Syllabus:

Cloud Architecture, Cloud Services Web-Based Application – Pros and Cons of Cloud Service Development, Types of Cloud Service Development, Centralizing Email Communications, Cloud Computing for the Community, Cloud Computing for the Corporation, Schedules and Task Management, Collaborating on Event Management – Collaborating on Contact Management, Collaborating on Databases – Storing and Sharing Files, Collaborating via Web-Based Communication Tools, Collaborating via Social Networks and Groupware – Collaborating via Blogs and Wikis.

Course Outcome:

After successful completion of the course, students should be able to:

- get a good understanding of cloud computing and a systematic knowledge of the fundamental technologies, architecture, and security. articulate the main concepts, key technologies, strengths, and limitations of cloud computing and the possible applications for state-of-the-art cloud computing
- identify the architecture and infrastructure of cloud computing, including SaaS, PaaS, IaaS, public cloud, private cloud, hybrid cloud, etc.
- explain the core issues of cloud computing such as security, privacy, and interoperability.
- choose the appropriate technologies, algorithms, and approaches for the related issues.
- identify problems, and explain, analyze, and evaluate various cloud computing solutions.

- provide the appropriate cloud computing solutions and recommendations according to the applications used.
- attempt to generate new ideas and innovations in cloud computing.

TEXT BOOKS:

1. Michael Miller, Cloud Computing: Web-Based Applications That Change the Way You Work and Collaborate Online, Que Publishing, 2008.

REFERENCES:

1. Dan C. Marinescu , Cloud computing: Theory and Practice, Morgan Kaufmann, 2013
2. Kai Hwang, Geoffrey C. Fox, Jack J. Dongarra, Distributed and Cloud Computing,: From Parallel Processing to the Internet of Things, 1/e, Morgan Kaufmann , 2011

In addition, manufacturers Device data sheets and application notes are to be referred to get practical and application oriented information.

Internal continuous assessment: 40 marks

Internal continuous assessment :
Test 1- 15 marks
Test 2- 15 marks
Assignment/Tutorial-10 marks
Total-40marks

COURSE PLAN:

Course No: 09EC7687 Title: **CLOUD COMPUTING** (L-T-P): 3-0-0 Credits: 3		
Modules	Hours	% marks in ESE
Module 1: Cloud Computing – History of Cloud Computing – Cloud Architecture – Cloud Storage – Why Cloud Computing Matters – Advantages of Cloud Computing – Disadvantages of Cloud Computing – Companies in the Cloud Today – Cloud Services Web-Based Application – Pros and Cons of Cloud Service Development – Types of Cloud Service Development – Software as a Service – Platform as a Service – Web Services – On-Demand Computing – Discovering Cloud Services Development Services and Tools – Amazon Ec2 – Google App Engine – IBM Clouds.	10	25
MODULE 2: Centralizing Email Communications – Collaborating on Schedules – Collaborating on To-Do Lists – Collaborating Contact Lists	7	13

FIRST INTERNAL TEST		
Cloud Computing for the Community – Collaborating on Group Projects and Events – Cloud Computing for the Corporation.	6	12
Module 3 Collaborating on Calendars, Schedules and Task Management – Exploring Online Scheduling Applications – Exploring Online Planning and Task Management – Collaborating on Event Management – Collaborating on Contact Management – Collaborating on Project Management – Collaborating on Word Processing - Collaborating on Databases – Storing and Sharing Files.	10	25
SECOND INTERNAL TEST		
Module 4 Collaborating via Web-Based Communication Tools – Evaluating Web Mail Services – Evaluating Web Conference Tools – Collaborating via Social Networks and Groupware – Collaborating via Blogs and Wikis.	9	25
END SEMESTER EXAMINATION		
Total Hours	**42**	

Course No: 09EC7663

Course Title: SEMINAR

Credits: 0-0-2: 2 **Year : 2015**

Pre-requisites: Nil

Objective:
To assess the debating capability of the student to present a technical topic. Also to impart training to students to face audience and present their ideas and thus creating in them self esteem and courage that are essential for engineers.

Syllabus:

Individual students are required to choose a topic of their interest from Embedded Systems related topics preferably from outside the M.Tech syllabus and give a seminar on that topic about 15 minutes. A committee consisting of at least three faculty members (preferably specialized in Embedded Systems) shall assess the presentation of the seminar and award marks to the students.

Each student shall submit two copies of a write up of his/her seminar topic. One copy shall be returned to the student after duly certifying it by the chairman of the assessing committee and the other will be kept in the departmental library. Internal continuous assessment marks are awarded based on the relevance of the topic, presentation skill, quality of the report and participation.

Course Outcome:

After successful completion of the seminar, students shall be able to

- Understand technical articles in peer reviewed journals and conferences
- Analyze and present advanced topics in Embedded Systems
- Their communication, presentation skills etc. shall be improved and shall be ready for technical paper writing.

Internal continuous assessment: 100 marks

Subject Relevance	:	10 marks
Concept/ Knowledge in the topic	:	20 marks
Presentation	:	40 marks
Report	:	30 marks
Total marks	:	**100 marks**

Course No: 09EC7683

Course Title: MASTER RESEARCH PROJECT PHASE I

Credits: 0-0-12: 6 Year : 2015

Pre-requisites: Nil

Objective:

- *To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.*

Syllabus:

The project work can be a design project/experimental project and/or computer simulation project on any of the topics in electronics design related topics. The project work is allotted individually on different topics. The students shall be encouraged to do their project work in the parent institute itself. If found essential, they may be permitted to continue their project outside the parent institute, subject to the conditions of M.Tech regulations. Department will constitute an Evaluation Committee to review the project work. The Evaluation committee shall be headed by the head of the department with two other faculty members in the area of the project, of which one shall be the project supervisor.

The student is required to undertake the master research project phase 1 during the third semester and the same is continued in the 4thsemester (Phase 2). Phase 1 consist of preliminary thesis work, two reviews of the work and the submission of preliminary report. First review would highlight the topic, objectives, methodology and expected results. Second review evaluates the progress of the work, preliminary report and scope of the work which is to be completed in the 4th semester. The Evaluation committee consists of at least three faculty members of which internal guide and another expert in the specified area of the project shall be two essential members.

Course Outcome:

After successful completion of the project phase I, students should be able to:

- Formulate a research problem and perform literature review
- systematically carrying out a research and write technical reports

Internal Continuous assessment: 50 Marks

	Supervisor/ Guide	Evaluation Committee
Project Review	**20 Marks**	**30 Marks**

FOURTH SEMESTER

Course No: 09EC7684

Course Title: MASTER RESEARCH PROJECT PHASE II

Credits: 0-0-21: 12 Year : 2015

Pre-requisites: Nil

Objective:

- *To improve the professional competency and research aptitude by touching the areas which otherwise not covered by theory or laboratory classes. The project work aims to develop the work practice in students to apply theoretical and practical tools/techniques to solve real life problems related to industry and current research.*

Syllabus:

Masters Research project phase-II is a continuation of project phase-I started in the third semester. Before the end of the fourth semester, there will be two reviews, one at middle of the fourth semester and other towards the end. In the first review, progress of the project work done is to be assessed. In the second review, the complete assessment (quality, quantum and authenticity) of the Thesis is to be evaluated. Both the reviews should be conducted by guide and Evaluation committee. This would be a pre qualifying exercise for the students for getting approval for the submission of the thesis.

At least one technical paper is to be prepared for possible publication in journal or conferences. The technical paper is to be submitted along with the thesis. The final evaluation of the project will be external evaluation.

Course outcome:

The students who successfully complete this course will have the demonstrated capability to

- Formulate a research problem in embedded systems area
- Systematically carrying out a research
- Write technical reports and research publications
- Publish research findings

Internal Continuous assessment: 100 Marks

	Supervisor/ Guide	External Expert	Evaluation Committee
Project Review	**30 Marks**	**30 Marks**	**40 Marks**