National Institute of Electronics and Information Technology Gorakhpur

Name of Group: Electronics Division.

Name of Course: VLSI Design using CADANCE Tool.

Objective:

Describe the different VLSI Technologies
Design the Digital circuits using Combinational and Sequential elements.
Draw the Layouts of Logical Cells and other logics.
Describe the different methodologies in System Design.

Duration: 4 Weeks / 6 Weeks

Eligibility: Students who have completed or pursuing B.E / B.Tech. / Diploma / ITI.

Course Fees: Rs. 1,000/- per week (+ GST)

Registration Process: Candidates have to apply in prescribed application form. The forms can be collected from NIELIT Gorakhpur centre. The duly filled form along with the course fees has to be submitted at NIELIT Gorakhpur centre. The Fees deposited is Non-Refundable.

Course Content:

Modules:	**Instruments and Measuring techniques to be covered.**
Module-1	Logic families, VLSI technology trends performance measures and Moore's law Comparisons of technology trends. Pass transistors and transmission gates. Implementation of Boolean functions and combinational circuits using switch logic & gate logic. Pseudo NMOS inverter, Dynamic and clocked CMOS inverters. Clocking strategies, single and tw0-phase clocking, clock distribution. Scaling of MOS circuits. Implementation of Boolean functions using basic gates synchronous and Asynchronous sequential circuits- Flip Flops.
Module-2	Project

* There will be 3 Hours Session per day.
* These sessions will include Theory Classes, Demo and Practical.

Mode of Payment: Fees can be paid either by swiping debit/credit card or by challan.

For any queries and more details please contact Sh. Deepam Dubey (**8317093874)**