NIELIT CHENNAI

List of Beneficiaries trained under SCSP/TSP scheme during April 2012 to March 2013

SCSP Scheme

S.No.	Student Name	Course Name
1	Prabakaran E	Information security L1
2	Joseph	Information security L1
3	Vivekananthan E	Web design using flash
4	M.Sathish Kumar	Digital Design using Verilog
5	Bharani	Web design using HTML & CSS
6	Shanmuganandam	Web design using HTML & CSS
7	M Prassanna venkadesh	Web design using HTML & CSS
8	Gajaraj Sekar G.K.	Digital Signal & Image Processing (ITA01C)
9	Rahul Bharath M.	Digital Signal & Image Processing (ITA01C)
10	Balaji D.	Digital ASIC Design & Verification; (VLE29)
11	Sathish Kumar	Digital ASIC Design & Verification; (VLE29)
12	Naresh V.	Matlab Programming (ITA25)
13	Vasanth S.	Embedded System Design
14	Priya Mohad	Embedded System Design
15	P.Nishanth	Embedded System Design
16	Parivallal S.	VLSI System Design & Verification
17	S.Naveen Prasanth	VLSI System Design & Verification
18	A.Kalaidasan	VLSI System Design & Verification
19	S.Kalpana	Graphics & Web designing
20	R.Akila	Graphics & Web designing
21	S.Karthikeyan	Graphics & Web designing
22	M.Gnana Prabu	Practical Automation using µC-L1 (VLE31)
23	D.Pugazhendhi	Practical Automation using µC-L1 (VLE31)
24	Roshni Priyaanka K.	Practical Automation using µC-L1 (VLE31)
25	S Muralidharan	FPGA Design & Board level debugging(VLE30)
26	D.Sundaramahalingam	FPGA Design and on-chip debugging(VLE30)
27	V.Vigneshwari	Programming through Java(ITN18)
28	M.Gnanaprabu	Programming through Java(ITN18)
29	M.K.Shyam Sunder	Data structures and programming using C(ITN19)
30	P.Nithiya	Data structures and programming using C(ITN19)
31	R.Ajith Kumar	Data structures and programming using C(ITN19)
32	Meganathan E.	Summer Projects (ITN21)
33	Ezhilarasan M.	Networking L1(ITN20)
34	R.Babu	Networking L1(ITN20)
35	T.Nepolean	Networking L1(ITN20)
36	S.Ramanan	Matlab Programming (ITA28)
37	Brijesh Kumar	Matlab Programming (ITA28)
38	M.S.Siranjeevi	Matlab Programming (ITA28)
39	M.Deepika Priyadarshini	Flash animation for content creation(ITA27)

40	S.Shanmuganandam	Flash animation for content creation(ITA27)
41	R.Rakesh	Flash animation for content creation(ITA27)
42	P.Senthamizh	ASIC Design & Verification using cadence EDA Tools(VLE33)
43	S.Manobalasaranya	ASIC Design & Verification using cadence EDA Tools(VLE33)
44	E.Vijay	ASIC Design & Verification using cadence EDA Tools(VLE33)
45	Balraj	Web design using HTML & CSS (ITA30)
46	Ganesh K.	Web design using HTML & CSS (ITA30)
47	Pushparaj T.	Web design using HTML & CSS (ITA30)
48	C.C.Kugan	Practical Automation using Arduino (VLE35)
49	D.Deepak	Verilog modelling & On-chip debugging(VLE34)
50	N.V.Sudharsan	Verilog modelling & On-chip debugging(VLE34)
51	N.Govindasamy	Verilog modelling & On-chip debugging(VLE34)
52	R.Thivakar	VLSI System Design & Verification (VLEM03)
53	V.Shobamanohari	VLSI System Design & Verification (VLEM03)
54	N.Priyanga	VLSI System Design & Verification (VLEM03)
55	V.Sheshavarma	Network Administration & Information Security
56	M.Kesavan	Network Administration & Information Security
57	K.Vijaya Kumar	Information Security using Virtual Training Environment(ITN22)
58	N.Prasanth	Information Security using Virtual Training Environment(ITN22)
59	B.Arun kumar	Information Security using Virtual Training Environment(ITN22)
60	L.Bhuvaneswari	Integrated Embedded & VLSI System Design
61	M.Kirubagari	Integrated Embedded & VLSI System Design
62	G.Kishore Kumar	Integrated Embedded & VLSI System Design
63	H.Bharath	Embedded System Design
64	R.Anbarasu	Embedded System Design
65	K.Santhosh Kumar	Embedded System Design
66	R.Rambo	VLSI System Design & Verification
67	A.Anand	VLSI System Design & Verification
68	H.Bharath	VLSI System Design & Verification
69	D.Balaji	ESD using Arduino & Beagle boards
70	T.Vinoth	Matlab programming
71	Rahul Bharath	DSP using MATLAB
72	Harikrishnan K.	VLSI System Design & Verification
73	M.Balaji	VLSI System Design & Verification
74	K.Pravin Kumar	Windows server administration
75	R.Nallathambi	Windows server administration
76	R.Sri Balaji	Windows server administration
77	R.Ashok Kumar	Hacking anatomy and counter measures
78	C.Babu	Hacking anatomy and counter measures
79	T.Deepika	Practical automation using 8051, ARM & LabVIEW

TSP Scheme

S.No.	Student Name	Course Name
1	Mushfiq Sarfaraz Yasin	FPGA Design and on-chip debugging(VLE30)