ONLINE INTERNSHIP PROGRAM
On
VLSI Design
Covering Analog and Digital Design Flow

Date: 14th SEPTEMBER-2020

Course Description:

This is an online, instructor – led course which provides a thorough knowledge about the VLSI Design, covering Analog and Digital Design Flows. The program consists of two weeks of online training and one week of extended lab support for the candidates. Well experienced faculties from National Institute of Technology (NIT Calicut) and National Institute of Electronics and Information Technology (NIELIT Calicut), will be handling the sessions for all the 10 Days.

Program Objectives

To learn & practice Analog and Digital industry standard VLSI Design methodologies. To get exposure in industry standard VLSI Design Tools and Flow.

Who can attend?

Students of Engineering (UG & PG) & MSc (Electronics), PhD scholars, faculty members and professionals from Industry.

Duration

- Proposed length of the training: 10 Days. 20 hours lectures 30 hours practicals.
- 1 week extended Lab support for practical sessions.

Course Fee
INR 1,500/- For students **INR 3,000/- For faculty** **REGISTER NOW** **INR 5,000/- For industry/corporate professionals** **Last date for payment and confirmation: 11-Sept-2020**

Payment Guidelines: -

Online fund transfer can be made via your Internet Banking / Google Pay to the following account and proof of the same has to be uploaded during the registration.

Account details:

Name of the Institute: National Institute of Electronics and Information Technology, Calicut.
Account Holder: Director NIELIT Calicut

Account No: 10401158037 Bank Name: SBI, NIT Chathamangalam

IFSC No: SBIN0002207 MICR Code: 673002012

For any queries WhatsApp to 9447769756, Please don't call, we will reply to you at the earliest.

Delivery Mode: Online. Live sessions /recorded classes, followed by online assignments over LMS. Students should have laptop/PC with high speed internet connectivity.

Tentative Schedule

Duration	:	2 weeks + 1 week extended practice sessions.
Tentative Timings	:	10 am to 12.00 noon (Theory) Lab/Assignments can be submitted online on Leaning management Systems (Any Time)
Tentative dates	:	14th September 2020

Syllabus

	Theory	LAB	Faculty (Indicative)
Day 1	MOSFET/small signal model/digital switch model/frequency of operation/region of operation (saturation)/CMOS technology – **1 hour** Current mirror, biasing, cascode current mirror- **1 hour**	MOSFET characteristics and current mirror	NIT Calicut
Day 2	CMOS inverters, static CMOS combinational circuits/any other digital circuit, dynamic circuits – **2 hours**	Inverter – schematic and layout	NIT Calicut
Day 3	Single stage amplifiers (CS, CD, cascode, folded cascode)/single stage op amp including folded cascode buffer- **2 hours**	CS amplifier	NIT Calicut
Day 4	Two stage op amp design and compensation – 2 hours	Two stage-op amp	NIT Calicut
Day 5	Two stage op amp design and compensation – **1 hour** Noise, mismatch, offset, linearity etc and layout in analog circuit design-**1 hour**	Two stage-op amp	NIT Calicut
Day 6	**Digital Logic Design using Verilog HDL I** Contents : Intro to Digital VLSI Design Flow Intro to Verilog HDL (IEEE 1364-2205) Design Abstractions Operators & Lexical Conventions, Design Examples	Simulation Lab Modelsim SE® Multiplexors, demultiplexors, Encoders, adders , parity generator etc **With assignments to be completed from candidate end.**	NIELIT Calicut

Day 7	Digital Logic Design using Verilog HDL II Hierarchical Modeling, Linear Test benches, Sequential logic design examples:	Simulation Lab(Modelsim SE®)Flip-flops, Counters, Waveform generators, FSM modeling etc **With assignments to be completed from candidate end.**	NIELIT Calicut
Day 8	Digital Logic Synthesis using EDA Tools-I (Basic of synthesis, introduction to fab files etc.)	Demo for Synthesis Lab- Cadence Genus/open source standards **With assignments to be completed from candidate end.**	NIELIT Calicut
Day 9	Digital Logic Synthesis using EDA Tools –II (Design considerations for Synthesis, SDC Writing, Synthesis Effort, Timing consideration etc.)	Synthesis Lab- Cadence Genus/open source standards **With assignments to be completed from candidate end.**	NIELIT Calicut
Day 10	RTL to GDSII Flow	Demo of flow in industry standard Tool Chain	NIELIT Calicut

Certificate: e-Certificate will be mailed to the registered email address after completion of the course.

Course Materials

Lectures Notes will be given to each participant via email/WhatsApp

Coordinators

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