COURSE PROSPECTUS

Name of the Group: ***VLSI Design Group***

Name of the Course: ***Certificate Program on System Verilog and UVM***

Course Code: ***VL800***

Starting Date: ***15th October 2018***

Duration: ***2 Months***

Course Coordinator: Sreejeesh SG, Mob: 9447769756 sree@calicut.nielit.in or sreejeesh@nielit.gov.in

Preamble:
SystemVerilog is the first industry-standard language covering the requirements of both design and verification. It provides the benefits of broad capability in all areas of design and verification, with the advantage of a widely supported IEEE standard spanning project generations. It's a massive language that breaks down into three separate blocks; the design language, assertions, and the testbench language.

This course on System Verilog and UVM how to get started with using SV as a language in Verification Scenario. It covers the basics of SV syntax, explains verification mechanisms including working with arrays, classes, matrices etc.

Objective of the Course:
The course teaches how to apply System Verilog to do verification and verification architecture design. It teaches System Verilog's key concepts such as data types, RTL design, Interfaces, clocking, assertion-based verification, and classes. The course provides a number of code samples and examples to give students a better feel for the language. It equips students to design a high performance IC or VLSI chip by imparting knowledge of all aspects of digital design, from architecture, application algorithm to fabrication.

Outcome of the Course: Skills Gained after completing this training, you will know how to:

- Describe the advantages and enhancements to SystemVerilog to support verification
- Define the new data types available in SystemVerilog
- Analyze and use the improvements to tasks and functions

- Discuss and use the various new verification building blocks available in SystemVerilog
- Describe object-oriented programming and create a class-based verification environment
- Explain the various methods for creating random data
- Create and utilize random data for generating stimulus to a DUT
- Identify how SystemVerilog enhances functional coverage for simulation verification
- Utilize assertions to quickly identify correct behavior in simulation
- Identify how the direct programming interface can be used with C/C++ in a verification environment.
- Understand the features and capabilities of the UVM environment for SystemVerilog

Course Structure: This course contains 2 modules. After completing the First module, the students have to do a 3 weeks project using any of the topics studied to earn the Certificate.

Other Contents

a. **Course Fees** :

General Candidates: Course fee is **Rs 25,000/- including GST**

SC/ST Candidates: Tuition Fees are waived for SC/ST students admitted under SCSP/TSP. However they are required to remit an amount of **Rs. *2500/-* as Advance caution/security deposit**. This amount will be considered as caution/security deposit and will be refunded after successful completion of the course. If the student fails to complete the course successfully this amount along with any other caution/security deposits by the student will be forfeited.

Modular wise Course Fee: Not Applicable for this course

VL800: Certificate Program on System Verilog and UVM			
Module & Course Code		**Module Name**	**Duration (Weeks)**
Module I	VL801	System Verilog and UVM	5
Module II	VL802	Project	3

b. **Registration Fee:** Nil

c. **Course Fee Installment Structure**:

Students can pay the full fees of ***Rs25, 000***/- - *(including GST*) in advance or as installments as given below

Fees	*Amount for General Candidates	Amount for SC/ST Candidates	Due Date (on or before)
1st Installment	Rs.25,000/-	Rs. 2500/-	**15th October 2018 {After the publication of selection list on 9th October you can pay the fees online to confirm your seats}**

* Above fees is inclusive GST@actuals (*18*%)

Eligibility: ME/M-Tech/B.E/B.Tech/B.Sc/MSc/Engineering Graduates/PG in Electrical/Electronics/Electronics &Communication/Bio-Medical Engineering/Medical Electronics/Electronics & Instrumentation/Computer Science and allied branches.

Prerequisites:

Knowledge in verilog HDL, C, C++, OOPS Concepts.

d. Number of Seats : 15
(SC/ST candidates and Persons with disabilities are eligible for seat reservation as per existing rules.)

How to Apply:

Students are advised to apply online @http://nielit.gov.in/content/online-registration. Payment towards fee of the course *may be paid through online payment gateway available in the Registration page or through any of the mode of payments specified in http://nielit.gov.in/calicut/content/mode-payments-0* after publication of Selection List

The Institute will not be responsible for any mistakes done by either the bank concerned or by the depositor while remitting the amount into our account.

Selection of candidates: *The selection to the course shall be based on the following criteria:*

i. Selection of candidates will be based on their marks in the qualifying examination (i.e. their B.Tech/M.Tech Marks) subject to eligibility and availability of seats.
ii. Knowledge in Verilog HDL Programming, C, C++ and Basic Electronics is a pre-requisite of this course.
iii. The list of Provisionally Selected Students will be published in our website http://nielit.gov.in/calicut on **9- October- 2018**

iv. All candidates who are provisionally selected have to **pay the full fee** on or before **15th October 2018**.

Selected candidates are requested to send the proof of remittance of fee, so as to reach the Centre by **15th October 2018, by email in sreejeesh@nielit.gov.in cc to trng@calicut.nielit.in**

e. Test/Interview (*if applicable*) : *Not applicable*

f. Counseling/Admission : ***15th October 2018***

g. Spot Admission: Unfilled/vacant seats are filled through spot admission. Spot admission (if open) will close within 15 days of Counseling/Admission of a particular course. On spot admission students should provide an undertaking saying that he/she is fully aware that he/she missed so much days of class and will not ask for extra classes or further extension of course. *(only 5 days for certificate courses)*

h. Admission Procedure :
Students who have been selected for test/interview/counseling/admission are required to report to the Institute on the prescribed day by 9:30 hrs along with the following

- **Original and attested Copies of Proof of Age, Qualifications, etc**
- **One passport size photograph and one stamp size photograph for identity card.**
- **SC/ST Certificate (Original and two attested copies, if applicable)**
- **Govt. issued photo id card (Aadhaar mandatory for SC/ST candidates. Original and one copy)**

i. Discontinuing the course: No fees (including the caution/security deposit) under any circumstances, shall be refunded in the event of a student discontinuing the course. No certificate shall be issued for the classes attended.

A student can however, be eligible for module certificates (applicable only for courses which provide for modular admission) which he has successfully completed provided, he/she has paid the entire course fees. This is not applicable to SC/ST candidates availing fee concession. SC/ST candidates availing fee concession are eligible for module certificates only after completing the full course with required attendance

j. Course Timings : **9.30 am to 5 pm**

k. Location and how to reach :
NIELIT Calicut is located very close to NIT campus and is about 22Kms from the Calicut (Kozhikode) city. A number of buses (Buses to NIT via Kunnamangalam) are available from "Palayam Bus Stand and KSRTC Bus

Stand". The bus stop at our Institute is called "Panthrand" and is one stop before NIT. The bus fare is around Rs.19/- from Calicut City to NIELIT.

Calicut (Kozhikode) is well connected by Rail, Road and Air form different parts of the country. The maximum and minimum temperatures range between 35^{0}C and 20^{o}C.

l. Course enquiries :
Students can enquire about the various courses either on telephone or by personal contact between 9.15 A.M. to 5.15 P.M. (Lunch time 1.00 pm to 1.30 pm) Monday to Friday.

m. **Important Dates :**

Events	***Dates***
Selection List Publication	**9th October 2018**
Counselling	***15th October 2018***
Class Starting	**16th October 2018**

Placement:

We have a placement cell, which provides placement assistance to students who qualify our courses. The course improves the knowledge and skill of the students as it deals with the latest technologies and tools used in industries. This helps the student in getting a placement by

a. Campus placement
b. Placement by companies for whom we send the students bio data and they conduct interviews at their site.

n. Students themselves attend interview at different companies and the course helps in the interview
o. You can visit our website and our official fb page for viewing the testimonials of our students.
https://www.facebook.com/pg/CAL.NIELIT/photos/?tab=album&album_id=977452965687163

p. **Hostel facilities :**

Hostel accommodation is available for boys and girls on monthly or daily chargeable basis. The hostel fee varies from Rs.1,400 /- to Rs.1,500/- per month depending on the type of accommodation. However, students are required to pay the hostel fees for the entire duration of the course for which they are seeking admission at the time of joining the course itself.

r. Boarding facilities :

Canteen & Mess facility is available for both boys & girls, students, those who avail mess facility should pay monthly mess fee @Rs.130/*- per day. An amount of Rs.1,000/- should be paid as mess advance to the Canteen Contractor at the time of joining the mess which will be adjusted in the last month mess fee.

**as per the present rate of contract agreement*

An amount of Rs.3,000/- should be paid as caution deposit (hostel & mess) at the time of joining the hostel which will be refunded/adjusted at the end of the course. For students not availing hostel facility, Rs.1,000/- will be the caution deposit

s. Lab Facilities

Altera & Xilinx Development Boards & Trainer Kits
Xilinx ISE, Altera Quartus II, NIOS II Trainer Kits
ASIC Design & Verification tools from Cadence.
ASIC Design & verification tools from Synopsys.
Complete range of Simulation, Synthesis Tools from Mentor Graphics
FPGA Design and Verification Tools
Hardware-Software Co-verification Tools
IC Nanometer Design Tools (Back end tools)
System Modeling Tools
Digital Storage & Mixed Signal Oscilloscopes
Logic Analyser & SMD Reworkstation

Course Contents:

♦ Course Overview
♦ System Verilog modeling concepts
♦ Data types, declarations, syntax rules
♦ Procedural blocks and assignments
♦ Programming statements
♦ Operators and operation rules
♦ Compound data types and packages
♦ System Verilog interface ports
♦ Verification constructs and testbench interfaces
♦ Verification timing using clocking blocks
♦ Object Oriented test benches
♦ Dynamic arrays and scoreboards
♦ Constrained random stimulus generation
♦ Functional coverage
♦ Synchronization (events, mailboxes, semaphores)
♦ Assertions overview
♦ UVM Environment Overview – One Case Study
- Project