PG Diploma in ASIC Design and Verification

Objective of the Course:

Education in Engineering Colleges and Universities are severely lagging in meeting VLSI Industry's specific needs, which creates a big gap between the Industry's requirements and the skills of the fresh engineering graduates. Post Graduate Diploma in ASIC Design and Verification is structured towards bridging this Industry-Academia gap by providing ASIC/VLSI Industry specific courses with focus on Advanced Technical and Personal Skill development.

The Course designed in consultation with the ASIC/VLSI industry experts with decades of experience working for various MNCs, builds on the basic concepts in ASIC Design and Verification, and then moves to Advanced ASIC development and Verification Techniques and Methodologies. The course transforms a raw engineering graduate into a capable ASIC Design and Verification professional with both technical and soft skills as required by the industry.

Learning Outcomes:

This course provides comprehensive understanding about the fundamental principles, methodologies and industry practices. This uniquely hybrid course makes the successful participants readily employable in multiple roles available in relevant industries. For people interested in entrepreneurships this would be an excellent launch pad. In addition the course also serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.

Expected Job Roles:

VLSI Design Engineer

Duration of the Course (in hours)	720 hrs /*24 Weeks*
Appr. Fees (INR):	Rs.68,000/- (Service Tax Extra)
Minimum eligibility criteria and prerequisites if any	a. M.E/M.Tech/BE /B.Tech in Electronics/ Electronics & Communication/ Electrical/ Instrumentation/ Computer Science/IT or M.Sc (Electronics). Diploma students may also be considered. b. Graduates with appropriate experience, Final year students, Candidates who have appeared in the qualifying examination and awaiting results may also apply.

Outline of the Course

S. No	Topic	Minimum No. of Hours
1.	Hardware Description Language-Verilog	90
2.	Functional Verification	60
3.	Advanced Verification Language-System Verilog	120
4.	Assertion based Verification	60
5.	Coverage driven Verification and Functional Coverage in SV	60
6.	DPI and Verification Methodology	120
7.	ASIC Prototyping	90
8.	Project	120
	Theory/ Lecture Hours:	216
	Practical/ Tutorial Lecture Hours:	504
	Total Hours:	720

Books recommended for
reference and reading:

1. A Verilog HDL Primer by J. Bhasker
2. Writing Testbenches using SystemVerilog by Janick Bergeron
3. Verification Methodology Manual by Janick Bergeron
4. SystemVerilog For Verification by Chris Spear

Group Code: VLSI

Group Name: VLSI

Course Code: PG02

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