B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FOUR** questions.

2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein. **(1x10)**

1.1 An arithmetic shift-right is equivalent to
A) multiplying the number by 2
B) dividing the number by 2
C) changing the sign of the number
D) reversing the number

1.2 The computer can be interrupted if
A) IEN= 0, FGI=0
B) IEN= 0, FGI=1
C) IEN= 1, FGI=0
D) IEN= 1, FGI=1

1.3 Suppose we have an instruction at address 021 with I=0, Opcode is of LDA and address part= 083, memory content at 083 = B8F2 and AC= A937. What will be the contents of AC after the execution? (all numbers are in Hexadecimal)
A) A832
B) B8F2
C) A937
D) 0083

1.4 Two instructions needed in the basic computer to set the flip-flop E to 0 are
A) CLA, CME
B) CLE, CMA
C) CLE, CME
D) CLA, CMA

1.5   Suppose A= 01000001 and B= 10000100. What will be the values of status bits C (borrow) and Z after evaluating (A-B) (assume signed-magnitude method):
A)   C=1, Z=0
B)   C=1, Z=1
C)   C=0, Z=1
D)   C=0, Z=0

1.6   In Booth's algorithm what is the operation performed if $Q_{n+1} = 1$, $Q_n = 0$
A)   shift-right
B)   add multiplicand and shift-right
C)   subtract multiplicand and shift-right
D)   no action

1.7   The register transfer statements for the interrupt cycle is
A) $T_0 T_1 T_2$ (IEN)(FGI $\wedge$ FGO) : R $\leftarrow$ 1
B) $T_0 T_1 T_2$ (IEN)(FGI $\wedge$ FGO) : R $\leftarrow$ 0
C) T_0 'T_1' 'T_2' (IEN)(FGI + FGO) : R $\leftarrow$ 0
D) T_0 'T_1' 'T_2' (IEN)(FGI + FGO) : R $\leftarrow$ 1

1.8   When a number is negative, the sign is represented by 1 but the rest of the number may be represented in one of the following ways:
A)   Signed-magnitude representation
B)   Signed-1's complement representation
C)   Signed-2's complement representation
D)   All of the above

1.9   The memory unit has a capacity of 8192 words of 32 bits/word. How many memory flip-flops are needed for the memory address register?
A)   12
B)   13
C)   14
D)   15

1.10   The micro-programmed control unit is
A)   potentially faster than hardwired
B)   linked to the introduction of low cost and high density memory chips
C)   much more flexible
D)   all of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein. (1x10)

2.1 An adder/subtractor single unit can be designed using full adder and XOR gates.

2.2 A sequential circuit is an interconnection of gates.

2.3 Hardwired control cannot be optimized to produce a fast mode of operations.

2.4 BSA is similar to BUN instruction.

2.5 Mask operation is an Exclusive OR operation.

2.6 J-K flip-flop is a combinational circuit.

2.7 In arithmetic shift operation, we need to consider the sign bit also.

2.8 RISC design approach reduces the average no. of clock cycles required to execute an instruction.

2.9 With memory-mapped I/O, all instructions that refer to I/O may also be used for reference to memory.

2.10 If the CPU and the I/O devices are controlled by different clocks, then it is Synchronous Communication.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1x10)

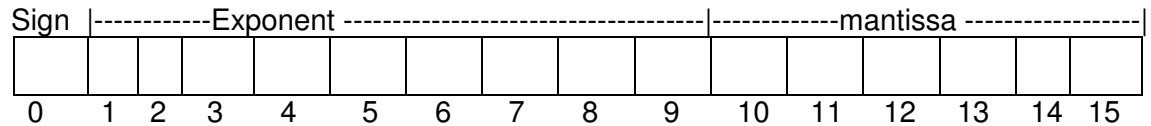| X		Y	
3.1	Virtual memory	**A.**	Flip-flop
3.2	Spooling	**B.**	Instruction specifies the fixed address
3.3	Memory-Mapped I/O	**C.**	Skip next instruction if the operand is not larger than the largest number
3.4	Associative memory	**D.**	Data are accessed by its contents
3.5	IEN	**E.**	Technique to reduce the speed mismatch between I/O devices and CPU
3.6	Indexed addressing	**F.**	Converts alphanumeric characters to binary codes
3.7	SPA	**G.**	Pure segmentation or Pure paging
3.8	Encoder	**H.**	Method of addressing I/O modules and external devices
3.9	Laser Printer	**I.**	A mode of data transfer
3.10	DMA	**J.**	Latch
		K.	Data selector
		L.	The fixed address is stored in a register
		M.	Non-Impact type printer

4. **Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein.** **(1x10)**

A.	Stack organization	**B.**	a': X = 0, b: X = X'	**C.**	Polling
D.	8	**E.**	32, 72	**F.**	4 bits
G.	Status register	**H.**	Blocks	**I.**	Spooling
J.	2 bits	**K.**	Control Words	**L.**	0010100
M.	16				

4.1   Functions for all micro-operations represented by strings of 1's and 0's are called _____.

4.2   If a computer use register window with Global registers=8, Local registers=8, Common registers=8 and no. of windows=4, then the window size and the total number of registers are _____.

4.3   A biased floating point number has 7 bits for a biased exponent and the bias constant = 64. Then the representation of exponent -24 is _____.

4.4   The overflow bit V is used to detect an arithmetic overflow in _____.

4.5   Zero address instructions are used in _____.

4.6   The RTL code for the transitions: if a=0 then X=0 ; if b=1 then X=X are _____.

4.7   The first _____ of a virtual memory address will specify the page number where the word is stored.

4.8   The number of chips required to provide a memory capacity of 2048 bytes for a computer that uses RAM chips of 1024 x 1 capacity =_____.

4.9   The fixed size groups of memory space are called _____.

4.10   _____ is a method of I/O handling by CPU.

5.
a)   Give 16 bit representation to represent the number -15.25 using the following format:

Sign |------------Exponent ------------------------------------|------------mantissa -----------------|

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

   i)   Bit 0 should be 0 if the number is positive and 1 if the number is negative.
   ii)   Exponent should be stored as number in 8th -complement form, (i.e., base=8)
b)   Evaluate the expression: a=(b +c)* d – e in 3 and 0-Address Machines.
c)   What is the significance of control functions? Design the complete hardware, including the logic gates for the control function that implement the statement:
   i) $xy' T_0 + T_1 + x'y T_2 : A \leftarrow A + 1$
   ii) $F T_1 + R' T_3 : A \leftarrow B$

(4+5+6)

6.
a)   i)   Convert 1A7 into decimal form.
   ii)   Explain logic circuit of D Flip-flop.
b)   Perform following arithmetic operations in binary using two's complement and 8-bit registers:
         $(14)_{10} – (5)_{10}$
c)   A digital computer has a memory unit with a capacity of 16,384 word, 40 bits per word. The instruction code format consists of 6 bits for the operation part and 14 bits for the address part. Two instructions are packed in the memory word, and a 40-bit instruction register IR is available in the control unit. Formulate a procedure for fetching and executing instructions for this computer.

(5+3+7)

7.
a)   The memory unit has a capacity of 8192 words of 32 bits per word.
   i)   How many flip-flops are needed for the memory address register and memory buffer register?
   ii)   How many words will the memory unit contain if the address register has 15 bits?
b)   Draw a flowchart for multiplication of two binary integers.
c)   Explain the following instructions:
   i)   Memory reference instruction.
   ii)   Register reference instruction.
   iii)   Input output instruction

(4+5+6)

8.
a)   Describe handshaking method for asynchronous data transfer.
b)   What do you mean by pipelining? Give an example of the same.
c)   Write an assembly language program to find the largest of 10 numbers.

(4+5+6)