A4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2. **PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

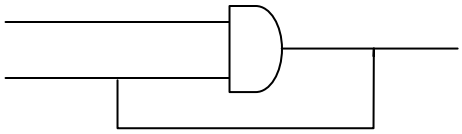
TOTAL TIME: 3 HOURS **TOTAL MARKS: 100**

(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1x10)

1.1 The circuit given below is



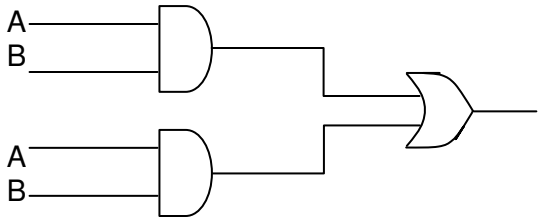
A) Combinational
B) Sequential
C) Hybrid
D) Analog

1.2 Which one of the following is universal gate?
A) AND
B) OR
C) NOR
D) NOT

1.3 In negative logic level 1 of the digital circuit is indicated by
A) 15v
B) 10v
C) 5v
D) 1v

1.4 An arithmetic shift-right is equivalent to
A) multiplying the number by 2
B) dividing the number by 2
C) changing the sign of the number
D) reversing the number

1.5 The output of the following circuit is



A) $\overline{A}\ \overline{B}$
B) AB
C) A
D) B

1.6 The following K-map solves to

	$\overline{A}$	A
$\overline{B}$	1	0
B	1	0

A) A
B) B
C) $\overline{A}$
D) $\overline{B}$

1.7 RAM is
A) Read and Add Memory
B) Random Access Memory
C) Rapid Access Memory
D) Redirected Address Bus Memory

1.8 A Computer has 64K memory starting from 0000. What is the last address of the memory?
A) 0FFF
B) FFFF
C) FFF0
D) None of the above

1.9 The fetch cycle is
A) first part of instruction cycle
B) last part of instruction cycle
C) intermediate part of instruction cycle
D) none of the above

1.10 The dedicated processor used for data transfer is
A) CPU
B) DMA
C) ALU
D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein. (1x10)

2.1 Offline device is connected to CPU.

2.2 The register transfer statement T_1:A ← A – B is implemented as A+ $\overline{B}$ +1.

2.3 In T_1+ T_2 : A ← B the '+' sign indicated addition of the timing values.

2.4 The postfix form of the expression (A+B)*(C+D) is AB+CD+*.

2.5 A stack organised computer does not use zero address instruction.

2.6 Hardware implementation of BSA instruction is used for handling interrupts.

2.7 In memory mapped I/O the addresses of memory and peripheral devices share the same address space.

2.8 Same clock pulse is used for asynchronous devices.

2.9 A buffer is needed in serial to parallel transfer mode.

2.10 Assembly language is a high level language.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1x10)

X		Y	
3.1	Two's complement of 0001111	**A.**	Paged Memory Management
3.2	2^n input and one output	**B.**	CISC
3.3	Exponent is baised and mantissa is normalized	**C.**	32
3.4	Number of symbols used is basic Hexadecimal number system	**D.**	Address modification
3.5	Fixed size instruction format	**E.**	Floating point
3.6	Fast memory	**F.**	Data transfer
3.7	Program of 4MB can be run on 1MB RAM	**G.**	12
3.8	Hand shaking	**H.**	1110001
3.9	Index Register	**I.**	RISC
3.10	BCD of 00110010	**J.**	16
		K.	Multiplexer
		L.	1110000
		M.	Cache memory

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein. (1x10)

A.	Bus interface	**B.**	Cache Memory	**C.**	Left
D.	Memory	**E.**	2^6 bytes	**F.**	Associative Memory
G.	Polling	**H.**	2^{17} bytes	**I.**	Parallelism
J.	2	**K.**	Software	**L.**	share same
M.	Right				

4.1 A clock pulse has _____ levels.

4.2 For multiplying a binary fixed point number by 2^4, shift _____ by four bits.

4.3 If the word size of memory is 2 bytes and address is of 16 bits, then the size of memory is _____ bytes.

4.4 _____ interrupt handles division by zero overflows.

4.5 Two synchronized devices _____ clock.

4.6 _____ is a method of I/O handling by CPU.

4.7 Pipelined architecture is used for implementing _____.

4.8 Content addressable memory is also known as _____.

4.9 The 8086 _____ is organised in two banks.

4.10 The 8086 has two units; Execution unit and _____ unit.

PART TWO

(Answer any **FOUR** questions)

5.

a) Draw logic diagram of 2x1 multiplexer. Using the block diagram of 2x1 multiplexer, give the design of 4x1 multiplexer.

b) Draw the logic diagram of J-K Flip flop and give its truth table and characteristic table.

(8+7)

6.

a) Explain the design of 4 bit binary down counter. Also, draw the diagram. Use T flip-flop.

b) Give addressing modes of a computer, which require access to the main memory.

(8+7)

7.

a) Use Booth's algorithm to multiply binary equivalent of $(11)_{10}$ and $(-13)_{10}$. Use 8 bits for representing the numbers.

b) How many address lines and input, output data lines are needed for a memory unit of 64K X 8 (where 64K is the number of words and word length is 8 bits).

(7+8)

8.

a) Explain the working of DMA transfer mechanism.

b) Describe working of cache.

(7+8)

9.

a) What are the various addressing modes of 8086? Explain each mode briefly.

b) Explain the four segment registers of 8086.

(8+7)