C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What is the difference between superscaling and pipelining?

b) Give three instruction formats of a basic computer.

c) Convert the following numbers with the indicated bases to decimal:

$(12121)_3$, $(4310)_5$,

d) A computer has a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

i) How many bits are there in the operation code, the register code part and the address part?

ii) What is the size of memory in MB units?

e) What is the basic difference between a branch instruction, a call subroutine instruction, and program interrupt?

f) A computer uses RAM chips of 1024Kb capacity. How many chips are needed to provide a memory capacity of 16K bytes? Explain in words how the chips are to be connected to the address bus.

g) Discuss the difference between tightly coupled multiprocessors and loosely coupled multiprocessors from the viewpoint of hardware organization and programming techniques.

(7×4)

2.

a) What is data dependency? Explain the types of data dependencies with suitable example.

b) Explain major characteristics of RISC and CISC.

c) Draw and specify the complete bit configuration of 8085 flag Register?

(8+6+4)

3.

a) What do you mean by instruction pipeline? Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

b) Explain cache mapping techniques in terms of cache memory.

c) Design 4-bit decrementer circuit using four full-adder circuits.

(8+6+4)

4.

a) What is direct memory access? Explain it's modes of operation.

b) Define the following terms:

i) Assembly language

ii) Bootstrap loader

iii) Program status word

(9+9)

5.

a) What are hazards in computer architecture? Explain data hazard with suitable example.
b) Explain register stack and memory stack organization in detail.
c) Draw the block diagram for 4 bit circuit for arithmetic/logic operators: add, subtract, AND, OR

(6+6+6)

6.

a) Give Flynn's Classification. Explain any two of them with suitable diagram.
b) Draw the flow chart of Booth algorithm for multiplication of singed-2's complement.
c) A CPU with a 20-MHz clock is connected to a memory unit whose access time is 40 ns. Formulate a read and write timing diagram using a READ strobe and a WRITE strobe. Include address in the timing diagram.

(8+6+4)

7.

a) Explain source-initiated transfer and destination-initiated transfer using handshaking.
b) What is content-addressable memory? Explain with its hardware organization.
c) Differentiate between hardwired control and micro programmed control. Draw the block diagram of a basic hardwired control organization with two decoders, a sequence counter and a number of control logic gates?

(6+6+6)