A4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1.	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2.	**PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3.	Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
                                                   (PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein. **(1x10)**

1.1 Conversion of hexadecimal number 6B2 to its binary number equivalent is
A) 111100011011
B) 011011010101
C) 011010110010
D) 011011000010

1.2 Which of the following registers is used to keep track of the address of the next instruction?
A) Memory Address Register
B) Instruction Register
C) Program Counter
D) Memory Data Register

1.3 The meaning of the instruction ISZ Y (increment and skip if zero) is
A) Increment the content of location Y by one, if the result is zero, skips the next instruction.
B) Increment the locations Y by one if it is zero then skip the next instruction
C) Increment the content of accumulator by one, if it is zero then skip to the location Y
D) None of the above

1.4 A better way to describe the operation of multiplexers is by means of a
A) Function Table
B) Truth Table
C) Symbol Table
D) Relation Table

1.5 Simplified form for Boolean Algebraic Expression F= ABC+ABC'+A'C (where A' means complement of A) is
A) BC+A'C
B) AB+A'C
C) AC+AC'
D) None of the above

1.6   A memory unit has 64 K words and each word is of 8 bits. How many address lines will be required in this case?
A)   16
B)   19
C)   6
D)   3

1.7   An arithmetic shift-left is equivalent to
A)   Multiplying the number by 2
B)   Dividing the number by 2
C)   Changing the sign of the number
D)   Reversing the number

1.8   In which addressing mode the operand is included in the instruction format?
A)   Indirect Addressing
B)   Direct Addressing
C)   Indexed Addressing
D)   Immediate Addressing

1.9   An instruction at address 016 with I=0, Opcode is of LDA and address part= 078,   memory content at 078 = C8D2 and AC= B8E7. What will be the contents of AC, after the execution? (All numbers are in Hexadecimal)
A)   C8D2
B)   A842
C)   B8E7
D)   F649

1.10   Solving the given Karnaugh's map results in expression
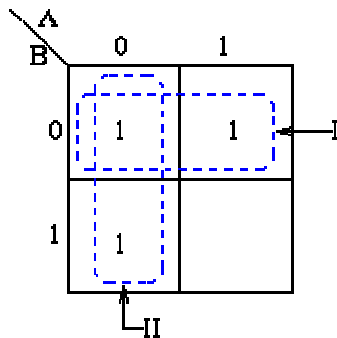
A' represents the complement of A.

A)   A'+B
B)   A+B'
C)   A+B
D)   A'+B'

2. **Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein.** (1x10)

2.1 Representation of the decimal number -16 in binary using two's complement is 11110010.

2.2 Making modifications are difficult in micro programmed control.

2.3 Control unit of the basic computer consists of two decoders, two sequence counters and a number of control logic gates.

2.4 During cycle stealing by DMA controller CPU remains inactive.

2.5 A decoder is a sequential circuit.

2.6 $A.A'=0$

2.7 The + symbol appearing in the following statement has the same meaning.

P+Q: R1 ← R2+R3 where P and Q are two binary variables of a control function.

2.8 Synchronous devices use same clock pulses.

2.9 Handshaking is a method of transmitting control signals between two independent units like CPU and I/O interface.

2.10 A stack-organized computer uses one address instruction format.

3. **Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein.** (1x10)

	X		Y
3.1	STA instruction	**A.**	Content Addressable Memory
3.2	2^n input and one output	**B.**	Combinatorial Circuit
3.3	Allows the execution of a program of size larger than the available memory	**C.**	D7
3.4	This changes by only one bit as it sequences from one number to the next	**D.**	CISC
3.5	Flip Flop	**E.**	Moves information from Accumulator to memory
3.6	A computer with large number of instructions	**F.**	Gray Code
3.7	It is used to increase the speed of processing	**G.**	Virtual memory
3.8	Determines the type of instruction in the decode phase of the instruction cycle	**H.**	1110001
3.9	Associative Memory	**I.**	Cache Memory
3.10	For every operation code the control unit issues	**J.**	16
		K.	Multiplexer
		L.	A sequence of micro operations
		M.	Auxiliary memory

4. **Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein.** **(1x10)**

A.	10010111	B.	Control Function	C.	CLA
D.	Memory mapped	E.	Z=0	F.	Adder-Subtractor
G.	Flip-flops	H.	2^{17}	I.	CMA
J.	Interrupt driven	K.	SIMD	L.	01100001
M.	MIMD				

4.1   The storage elements employed in clocked sequential circuits are called _____.

4.2   Binary Coded Decimal representation of decimal number 97 is _____.

4.3   If the word size of memory is 2 bytes and address is of 16 bits, then the size of memory is _____ bytes.

4.4   P is a _____ in the register transfer operation P: R2 ← R1.

4.5   Including an exclusive-OR gate with each full-adder results in _____.

4.6   The condition tested for Branch if not zero(BNZ) is _____.

4.7   _____ represents an organization that includes many processing units under the supervision of a common control unit.

4.8   In assembly language instruction field for complement accumulator is _____.

4.9   _____ I/O is better than programmed I/O.

4.10   _____ I/O does not distinguished between memory and I/O addresses.

5.
a) Perform the operation 13250 – 72532 of two unsigned decimal numbers using 10's complement. Explain each step clearly.
b) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?
c) Draw the logic diagram of a 2-to-4 line decoder using only NOR gates. Include an enable input. Write the complete truth table also.

(4+4+7)

6.
a) Given the Boolean function F= xy'z+x'y'z+xyz. Simplify the algebraic expression using Boolean algebra and draw the logic diagram from the simplified expression. Find out the reduction in number of gates.
b) The 8-bit registers AR, BR, CR and DR initially have the following values:
AR=11110010   BR= 11111111   CR=10111001   DR=11101010
Determine the 8-bit values in each register after the execution of the following sequence of micro operations

AR ←AR+BR   Add BR to AR
CR ← CR ^ DR, BR ← BR+1   AND DR to CR, increment BR
AR ←AR – CR   Subtract CR from AR

(9+6)

7.
a) With the help of flow chart explain how the control unit determines that a given instruction is a memory reference instruction, register reference instruction or input output instruction.
b) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of 7 addressing modes, a register address field to specify one of 60 processor registers and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.

(9+6)

8.
a) Explain the following terms in the context of Cache Memory:
  i) Locality of reference
  ii) Hit/Miss Ratio
  iii) Mapping
b) How many 128x8 RAM chips are needed to provide a memory capacity of 2048 bytes? Explain clearly.
c) Differentiate between programmed and interrupt driven I/O.

(6+4+5)

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9.
a) Write 8086 assembly language instructions to evaluate the arithmetic expression 5+(6-2) leaving the result in ax using (i) 1 register, (ii) 2 registers.
b) Write short notes on:
  i) DMA
  ii) Asynchronous Data Transfer

(8+7)