B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.

2. **PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.

3. Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS **TOTAL MARKS: 100**

(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 The no. of minterms in a truth table of n variables
A) n^2
B) 2^n
C) 2*n
D) n!

1.2 The algebraic function for XOR logic gate with two inputs A and B is
A) AA' + BB'
B) A(A+B)
C) AB+A'B'
D) A'B+AB'

1.3 The Octal equivalent of the Hexa decimal number A277 is
A) 121167
B) 504731
C) 5277
D) 7725

1.4 The value of register R, which contains 10000110, after Arithmetic Shift Right operation
A) 01000011
B) 00001100
C) 00001101
D) 11000011

1.5 The condition to detect overflow during the addition of two binary numbers is
A) C_n XOR C_{n-1}
B) C_n NOR C_{n-1}
C) C_n OR C_{n-1}
D) C_n AND C_{n-1}

1.6 Which of the following is not associated with DMA
A) Bus Request
B) Burst transfer
C) Programmed I/O
D) Cycle Stealing

1.7 DMA stops further transfer when
A) Control register contains zero
B) Address register contains zero
C) Word Count register contains zero
D) Control register contains one

1.8 If there are 8 words in cache memory and 32 words are in main memory, the number of bits used for the tag field of direct mapping organization is:
A) 3
B) 5
C) 2
D) 8

1.9 Given a 256*4 RAM chips, how many chips are required to provide a memory capacity of 1 KB of RAM.
A) 1
B) 8
C) 4
D) None of the above

1.10 How many lines of address bus must be used to access the memory made up of 4 chips of the capacity 256*16?
A) 4
B) 16
C) 14
D) 10

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 A full-adder is a combinational circuit having two outputs.
2.2 The ROM does not need a read-control line.
2.3 Internal interrupt are also called traps.
2.4 The memory mapped I/O uses the different address space for both memory and I/O.
2.5 Strobe control method of asynchronous data transfer overcomes the problem of acknowledgment faced by handshaking.
2.6 The last bit called the stop bit in serial asynchronous data transmission is always 1.
2.7 DI contains offset from the ES register only.
2.8 A segment register is used as a base location in all references to memory.
2.9 CISC machine/processor executes one instruction per clock cycle always.
2.10 DEC N, a pseudo instruction for the assembler, decrements the content of N by 1.

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

X		Y	
3.1	Two representation of zero	**A.**	Data transfer
3.2	Control function	**B.**	Page replacement
3.3	Register reference	**C.**	1's complement
3.4	AB+	**D.**	Virtual addresses
3.5	Relative addressing mode	**E.**	Data Transfer Instruction
3.6	JMP	**F.**	Program Control Instruction
3.7	LRU	**G.**	Program Counter
3.8	Address Space	**H.**	Opcode=111, I=0
3.9	Three-state gate	**I.**	Index Register
3.10	DMA	**J.**	High-impedance
		K.	2's complement
		L.	Boolean variable
		M.	Reverse Polish Notation

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	PSW	**B.**	Polling	**C.**	ROM
D.	throughput	**E.**	Decoders	**F.**	1Bh
G.	CDh	**H.**	Counter	**I.**	0 (Zero)
J.	Hit ratio	**K.**	1 (One)	**L.**	Flip-flop
M.	Macro				

4.1 When S and R are equal to _____, the output is unpredictable.
4.2 A _____ is a combinational circuit that converts binary information from the n inputs to a maximum of 2n unique outputs.
4.3 A register that goes through a predetermined sequence of states upon the application of input pulses is called a _____.
4.4 A _____ procedure is used to identify the highest-priority source by software means.
4.5 The performance of cache memory is frequently measured in terms of a quantity called _____.
4.6 The AX register contains 0000h. If we move 1BCDh to AX, AL register will be changed to _____.
4.7 The body of _____ is expanded in program at each place it is used.
4.8 The status bit in _____ can be used to detect whether CPU is working in supervisor mode or user mode.
4.9 The bootstrap loader is stored in _____.
4.10 The _____ status bit is used for testing if the result of an ALU operation is equal to zero or not.

PART TWO

(Answer **ALL** questions)

5.

a) Explain in brief JK Flip-Flop along with its graphic symbol and characteristic table. How is it different than SR Flip-Flop?

b) What is multiplexer? Draw a figure for 2-to-1-line multiplexer. Give its truth table and function table.

c) Give formula for r's complement and (r-1)'s complement for a number N in base r having n digits. Perform and explain 2's complement addition on following pair of numbers:
   i) -5, +14
   ii) +5, -14
   iii) -5, -14

(5+5+5)

6.

a) Draw and explain 4-bit adder-subtractor circuit.

b) An instruction is stored at location100 with its address field at location 110. The address field has the value 300. The value at location 200 is 300, at 300 is 400, and at 400 is 500. Draw memory diagram to describe this data. Evaluate the effective address and the operand if the addressing mode of the instruction is (i) Direct (ii) Indirect, and (iii) Immediate.

c) Describe the Associative Mapping organization of Cache Memory.

(5+6+4)

7.

a) Assuming suitable register and instruction set, give the sequence of instructions to evaluate the instruction E=(A+B)*(C+D) using following CPU organization:
   i) Single Accumulator
   ii) General register organization with two address instruction
   iii) General register organization with three address instruction
   iv) Stack organization

b) What is disadvantage of Strobe method? Explain in brief source-initiated data transfer procedure using handshaking along with its Block diagram and Timing diagram.

(8+7)

8.

a) Draw flow chart for Booth algorithm for multiplication of signed 2's complement numbers and explain step by step multiplication of (-9) and (-13).

b) Write an assembly language program to find the frequency of the character '.' in the text available at TEXT and put the result (frequency) at FREQ defined as word. The end of string in TEXT is encountered on finding '#'.

(10+5)