C0-R4.B4 : COMPUTER SYSTEM ARCHITECTURE

NOTE :

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1. (a) Considering r as the base, what is (r-1)'s complement of following numbers ?
   (i) $(231)_{10}$
   (ii) $(101)_3$
   (iii) $(101)_4$
   (iv) $(231)_8$
   (b) Define write-through and write-back methods.
   (c) Describe tightly coupled multiprocessor and loosely coupled multiprocessor.
   (d) List any four registers with their symbol and function.
   (e) Draw block diagram for 4-bit adder-subtractor and explain in brief.
   (f) The purpose of interface is to resolve the differences that exist between the CPU and each peripheral. List out those major differences.
   (g) What is pipeline processing ? List out the conflicts in instruction pipeline and explain each one of them in brief.

(7×4)

2. (a) Draw flowchart of Booth Algorithm for multiplication of two numbers and show step by step multiplication process of Multiplier: $(-7)_{10}$ andMultiplicand: $(12)_{10}$.
   (b) Classify shiftmicrooperations and explain each in detail. (Note: Hardware implementation is not required)

(10+8)

3. (a) Draw and explain flowchart for floating–point multiplication.
   (b) Consider 1MB of cache memory and 4 GB of main memory are partitioned into the blocks of 64KB. Word size is 2B. (Note: Memory is word addressable.)
      (i) How many bits are required for physical address ?
      (ii) How many block are there in main memory and cache memory ?
      (iii) How many bits are required for word offset ?
      (iv) How many TAG bits are required for
         (I) Direct Mapping
         (II) Associative Mapping
         (III) 4-Way Set Associative Mapping
   (c) List out the characteristics of CISC and RISC architecture.

(6+6+6)

4. (a) Draw the diagram of common bus system for four register and explain how register is selected by bus.

(b) What is the interrupt ? Explain External, Internal and Software interrupts in brief.

(c) Write and explain various hardware techniques to minimize performance degradation caused by Branch Instruction in pipeline.

(6+7+5)

5. (a) Explain RAM and ROM chips with its block diagram.

(b) Give details about SISD, SIMD and MIMD architectures.

(c) Define following terms:

(i) Machine language

(ii) Assembly language

(8+6+4)

6. (a) Write a program to evaluate the arithmetic statement X = (A + B) * (C + D) using zero address, one address, two address and three address instructions. Use ADD, SUB, MUL and DIV for four arithmetic operations; MOV for the transfer-type operation; and LOAD and STORE for transfer to and from memory and AC register. We will assume that the operands are in memory addresses A, B, C and D. Result must be stored in memory at address X.

(b) Explain arithmetic pipeline for floating point addition and subtraction with proper diagram.

(10+8)

7. (a) Draw the flowchart for interrupt cycle and explain it.

(b) How DMA transfer takes place in a computer system? Explain with proper block diagram.

(c) Perform following:

(i) Convert $(101011010)_2$ into octal.

(ii) Convert $(101011010)_2$ into hexadecimal.

(iii) Convert $(4352)_8$ into hexadecimal.

(iv) Convert $(31)_{10}$ into binary.

(6+8+4)