A4-R4/B1.4-R4 : COMPUTER SYSTEM ARCHITECTURE

अवधि : 03 घंटे
DURATION : 03 Hours

अधिकतम अंक : 100
MAXIMUM MARKS : 100

ओएमआर शीट सं. : OMR Sheet No. :					

रोल नं. : Roll No. :

उत्तर-पुस्तिका सं. : Answer Sheet No. :

परीक्षार्थी का नाम :
Name of Candidate : _____

परीक्षार्थी के हस्ताक्षर :
Signature of Candidate : _____

परीक्षार्थियों के लिए निर्देश :	**Instructions for Candidate :**
कृपया प्रश्न-पुस्तिका, ओएमआर शीट एवं उत्तर-पुस्तिका में दिये गए निर्देशों को ध्यानपूर्वक पढ़ें।	Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.
प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी केवल अंग्रेजी भाषा में ही उत्तर दे सकता है।	Question Paper is in English language. Candidate can answer in English language only.
इस मॉड्यूल/पेपर के **दो भाग** हैं। **भाग एक** में **चार** प्रश्न और **भाग दो** में **पाँच** प्रश्न हैं।	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
भाग एक ''वैकल्पिक'' प्रकार का है जिसके कुल अंक 40 है तथा **भाग दो** ''व्यक्तिपरक'' प्रकार का है और इसके कुल अंक 60 है।	**PART ONE** is Objective type and carries 40 Marks. **PART TWO** is Subjective type and carries 60 Marks.
भाग एक के उत्तर, **ओएमआर उत्तर-पुस्तिका** पर ही दिये जाने हैं। **भाग दो** की उत्तर-पुस्तिका में **भाग एक** के उत्तर **नहीं** दिये जाने चाहिए।	**PART ONE** is to be answered in the **OMR ANSWER SHEET** only. **PART ONE** is **NOT** to be answered in the answer book for **PART TWO**.
भाग एक के लिए अधिकतम समय सीमा **एक घण्टा** निर्धारित की गई है। **भाग दो** की उत्तर-पुस्तिका, **भाग एक** की उत्तर-पुस्तिका जमा कराने के पश्चात् दी जाएगी। तथापि, निर्धारित एक घंटे से पहले **भाग एक** पूरा करने वाले परीक्षार्थी **भाग एक** की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरंत बाद, **भाग दो** की उत्तर-पुस्तिका ले सकते हैं।	Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the Answer Sheet for **PART ONE** is returned. However, Candidates who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the Answer Sheet for **PART ONE** to the Invigilator.
परीक्षार्थी, उपस्थिति-पत्रिका पर हस्ताक्षर किए बिना और अपनी उत्तर-पुस्तिका, निरीक्षक को सौंपे बिना, परीक्षा हॉल/कमरा नहीं छोड़ सकते हैं। ऐसा नहीं करने पर, परीक्षार्थी को इस मॉड्यूल/पेपर में अयोग्य घोषित कर दिया जाएगा।	**Candidate cannot leave the examination hall/room without signing on the attendance sheet and handing over his/her Answer Sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.**
प्रश्न-पुस्तिका को खोलने के निर्देश मिलने के पश्चात् एवं उत्तर लिखना आरम्भ करने से पहले उम्मीदवार जाँच कर यह सुनिश्चित कर लें कि प्रश्न-पुस्तिका प्रत्येक दृष्टि से संपूर्ण है।	After receiving the instruction to open the booklet and before starting to answer the questions, the candidate should ensure that the Question Booklet is complete in all respect.

जब तक आपसे कहा न जाए, तब तक प्रश्न-पुस्तिका न खोलें।
DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.

PART ONE

(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet attached to the question paper, following instructions therein. **(1x10)**

1.1 Which flag will be set (1) if the result of a signed operation is too large to fit in the number of bits available to represent it, otherwise reset (0) in 8086 Microprocessor ?

(A) Carry flag

(B) Sign flag

(C) Overflow flag

(D) None of the above

1.2 The high impedance state is used in bus system constructed with :

(A) multiplexer

(B) two state gates

(C) three-state gates

(D) none of the above

1.3 A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates ?

(A) AND or OR gates

(B) NOR or NAND gates

(C) Both of above

(D) None of the above

1.4 Conversion of hexadecimal number A4E to its octal number equivalent is :

(A) 5116

(B) 6115

(C) 2638

(D) 10414

1.5 Which of the following memories must be refreshed many times per second ?

(A) Static RAM

(B) Dynamic RAM

(C) EPROM

(D) None of the above

1.6 When an instruction itself contains the operand (data) rather than the address of the operand, the technique is known as _____ addressing.

(A) Direct

(B) Indirect

(C) Immediate

(D) None of the above

1.7 In 8086 processor the size of prefetch queue is _____ bytes.

(A) 6

(B) 8

(C) 12

(D) 10

1.8 The minimum time delay between two successive memories read operations is _____.

(A) Latency

(B) Cycle time

(C) Delay

(D) None of the above

1.9 The minterm expansion of f(P, Q, R) = PQ + QR′ + PR′ is :

(A) m0 + m1 + m3 + m5

(B) m0 + m1 + m6 + m7

(C) m2 + m3 + m4 + m5

(D) m2 + m4 + m6 + m7

1.10 A XOR gate is ON only when all its inputs are :

(A) ON

(B) LOW

(C) OFF

(D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "OMR" sheet attached to the question paper, following instructions therein.

(1x10)

2.1 The output depends both on the current inputs as well as on how it got to the current state in combinational circuit.

2.2 The '1' in the MSB position indicates a negative number after adding two positive numbers.

2.3 Both segments register DS and ES point to the address of data.

2.4 ES is a spare segment that may be used for specifying a location in memory in 8086 assembly language.

2.5 The performance of cache memory is measured by Latency ratio.

2.6 The register which receives the information from output bus in CPU is selected by Program Counter.

2.7 Exclusive-OR gates can be used to generate a parity check bit.

2.8 The way the operands are chosen during program execution is dependent on the addressing mode of the instruction.

2.9 Two's complement of 1100110 is 0011011.

2.10 Pipelining is the process of accumulating instruction from the processor through a pipeline.

3. **Match words and phrases in column X with the closest related meaning/word(s)/phrases in column Y. Enter your selection in the "OMR" answer sheet attached to the question paper, following instructions therein.**

(1x10)

	X		Y
3.1	CPU fetches the instruction from the memory according to the value of	**A.**	8421
3.2	Stack Pointer	**B.**	Faster to access than RAM
3.3	Virtual Memory	**C.**	An illusion of an extremely large memory
3.4	EBCDIC	**D.**	Many input one output
3.5	Digital circuit generating arithmetic sum of two binary numbers of any length	**E.**	Full Adder
3.6	BCD is also known as	**F.**	One input many output
3.7	In Hardware algorithm for multiplication, the sequence counter contains initially	**G.**	RISC
3.8	Cache memory	**H.**	Address of the top element of the stack
3.9	Reduce the cycles per instruction at the cost of the number of instructions per program.	**I.**	The number of bits in multiplier
3.10	Multiplexer	**J.**	An extremely large main memory
		K.	Extended Binary Coded Decimal Interchange Code
		L.	Program Counter
		M.	Binary adder

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "OMR" answer sheet attached to the question paper, following instructions therein.

(1x10)

A.	99	**B.**	Push Down Stack	**C.**	Reverse Polish Notation
D.	Read	**E.**	5+[R1]+[R2]	**F.**	Absorption Law
G.	Synchronous	**H.**	Multiplying the number by 2	**I.**	Commutative Law
J.	Prefix	**K.**	Memory Stack	**L.**	4
M.	Write				

4.1 _____ OR gates are required for a Decimal-to-bcd encoder.

4.2 MN-PQ*+ is _____ form of an arithmetic expression.

4.3 An Arithmetic shift left is _____.

4.4 The time interval between two characters is fixed and constant while data transmission is _____ Data Transmission.

4.5 The effective address of the following instruction is MUL 5(R1,R2).

4.6 In case of, Zero-address instruction method the operands are stored in _____.

4.7 The transfer of information from a memory word to the outside environment is called a _____ operation.

4.8 The expression x + xy = x is called _____.

4.9 The PUSH and POP instruction transfer data between processor registers and _____.

4.10 Decimal number equivalent to 1100011 is _____.

PART TWO

(Answer any four questions)

5. (a) Explain DMA in detail with the help of diagram.

(b) Write an assembly language code to multiply two 8 bit numbers.

(8+7)

6. (a) Draw the logic diagram of a 2-to-4 line decoder using only NOR gates and prepare the truth table for the same. Include an enable input.

(b) Explain Memory mapped I/O.

(c) Describe the associative mapping organization of Cache Memory.

(7+3+5)

7. (a) Multiply the (+15) with (-13) using Booth's algorithm. Give each step.

(b) Write a basic difference between a S-R flip flop and JK flip flop.

(c) Explain various types of interrupts.

(6+4+5)

8. (a) Explain Parallel Adder/ Subtractor circuit.

(b) Describe any 5 addressing modes used in Basic Computer.

(c) Simplify the following Boolean functions, using four-variable maps.

$F(w, x, y, z) = \Sigma (1, 4, 5, 6, 12, 14, 15)$

(5+5+5)

9. Write short notes on **any three** :

(a) Asynchronous Data Transfer

(b) Virtual Memory

(c) RISC vs. CISC computers

(d) Interrupt Initiated I/O

(e) Instruction Pipelining

(5+5+5)

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SPACE FOR ROUGH WORK

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