B1.4-R4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1.	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
2.	**PART ONE** is to be answered in the **TEAR-OFF ANSWER SHEET** only, attached to the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book.
3.	Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates, who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE**.

TOTAL TIME: 3 HOURS   **TOTAL MARKS: 100**
(PART ONE – 40; PART TWO – 60)

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "tear-off" answer sheet attached to the question paper, following instructions therein. **(1x10)**

1.1 The hardware which is responsible for executing machine language instructions can be built using large number of few basic building blocks, which are called
A) Control Unit
B) CPU
C) Logic gates
D) None of the above

1.2 The output depends both on the current inputs as well as on how it got to the current state in
A) Combinational circuits
B) Sequential circuits
C) In both – combinational and sequential circuits
D) None of the above

1.3 The high impedance state is used in bus system constructed with
A) multiplexer
B) two state gates
C) three-state gates
D) none of the above

1.4 In indirect address mode, the operand part of the instruction contains
A) operand
B) address of the operand
C) address of the memory word which contains the address of the operand
D) none of the above

1.5 The register which receives the information from output bus in CPU is selected by
A) Decoder
B) IR
C) Program Counter
D) None of the above

1.6   Booth's algorithm is used
A)   To predict the result of the expression
B)   To add or subtract numbers
C)   To multiply two numbers
D)   None of the above

1.7   In handshaking method for transferring data from one unit to another unit
A)   Source unit initiating data transfer has no way of knowing whether destination unit has received it or not
B)   Two control lines are used
C)   Only destination unit uses one control line
D)   None of the above

1.8   Cycle stealing technique is associated with
A)   Asynchronous data transfer
B)   DMA transfer
C)   Synchronous serial data transfer
D)   None of the above

1.9   The program whose function is to start the operation of computer software when power is turned on is called
A)   Operating system
B)   System software
C)   Bootstrap loader
D)   None of the above

1.10   Virtual memory refers to computer system
A)   which allows to run even programs of size greater than the actual size of memory.
B)   which does not have any memory.
C)   which is capable of running the programs even when actual memory is damaged.
D)   none of the above.

2. **Each statement below is either TRUE or FALSE. Choose the most appropriate one and ENTER in the "tear-off" sheet attached to the question paper, following instructions therein.** (1x10)

2.1 Same number of transistors is required to implement **NOT** gate and **AND** gate.

2.2 Signed 1's complement method has two representation of zero.

2.3 Shift micro-operations are used for serial transfer of data.

2.4 Special character can not be the part of instruction.

2.5 '**Zero address**' instruction does not have address field.

2.6 Divide overflow condition during arithmetic operation always results in stopping of computer.

2.7 During DMA transfer, CPU is idle.

2.8 The I/O read and I/O write control lines are disabled during an I/O transfer.

2.9 Dynamic RAM offers reduced power consumption and large storage capacity in single memory chip.

2.10 Machine code is generated for every assembly language instruction.

3. **Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "tear-off" answer sheet attached to the question paper, following instructions therein.** (1x10)

	X		Y
3.1	A graphical method for simplifying logical expression	**A.**	Binary adder
3.2	Non-zero most significant digit of the mantissa (floating point representation)	**B.**	Associative Memory
3.3	Digital circuit generating arithmetic sum of two binary numbers of any length	**C.**	Static RAM
3.4	Basic component of arithmetic circuit	**D.**	Time out
3.5	Supervisor call instruction	**E.**	Hit ratio
3.6	Statement of solution of the problem by finite number of well defined procedure steps	**F.**	Dynamic RAM
3.7	Rate at which signal level changes	**G.**	Karnaugh Map method
3.8	Detecting incomplete data transfer	**H.**	Baud rate
3.9	The performance of cache memory	**I.**	Parallel adder
3.10	Content addressable memory	**J.**	Algebraic manipulation method
		K.	Normalized
		L.	Software interrupt
		M.	Algorithm

4. **Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Enter your choice in the "tear-off" answer sheet attached to the question paper, following instructions therein.** **(1x10)**

A.	synchronous	B.	ALU	C.	branch
D.	associative	E.	asynchronous	F.	NOT
G.	register	H.	shift	I.	3
J.	n	K.	segment	L.	2
M.	Start and stop bits				

4.1 Sequential execution of instructions can be changed by the use of _____ instruction.

4.2 Logical instructions perform binary operations on strings of bits stored in _____.

4.3 Multiplying an unsigned number stored in register by 2^n is equivalent to shifting _____ bits of register towards left.

4.4 _____ are used in serial asynchronous data transfer.

4.5 The _____ logical operator has got highest precedence.

4.6 The **AND** and **OR** gate implementation require only _____ transistors.

4.7 In _____, entire register transfer operation from source register and into destination register can be performed in one clock period.

4.8 In _____ transmission, two units share common clock frequency and bits are transmitted continuously.

4.9 _____ memories are expensive compared to random access memory.

4.10 The _____ registers are used in assembly language of Intel 8086 machine.

PART TWO
(Answer any **FOUR** questions)

5.
a) Explain the construction with logic diagram of a 4 – 1 line multiplexer
b) Comment on "Basic difference between a S-R flip flop and JK flip flop".
c) Explain how floating point representation of number is done? When do you say the floating point number is normalized? Represent the number $(+46.25)_{10}$ as floating point binary number with 32 bits.

(6+4+5)

6.
a) Obtain the simplified Boolean function of the full adder in the sum of product form and draw the logic diagram using NAND gate.
b) A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts:
- an indirect bit
- an operation code
- a register code part to specify one of 64 register and
- an address part

i) How many bits are there in op code, the register code part and address part?
ii) Draw instruction word format and indicate the number of bits in each part.
iii) How many bits are there in data and address input of the memory?
c) What is addressing mode? Why do computers use addressing mode techniques? Explain two modes with examples, which do not use address fields.

(6+[3x2]+3)

7.
a) Define program interrupt. What happens when an interrupt take place? How are these interrupts handled? Explain different types of the interrupts.
b) Explain Hardware Multiply algorithm through flow chart.

(9+6)

8.
a) Name the segment registers used in Intel 8086 Assembly language and mention the purpose of each register.
b) Write an assembly language code to count the number of bits on (i.e. which has value 1) in register AX.
c) Ten consecutive locations, defined as word, starting from WORD have signed numbers. Write an assembly language codes to find out how many numbers are odd and put the result at ODDNO.

(4+5+6)

9. Write short notes on:
a) DMA Transfer in computer
b) Virtual memory

(7+8)