A4-R4: COMPUTER SYSTEM ARCHITECTURE

अवधि: 03 घंटे **अधिकतम अंक: 100**
DURATION: 03 Hours **MAXIMUM MARKS: 100**

ओएमआर शीट सं.: **OMR Sheet No.:**						

रोल नं.: **Roll No.:** | | | | | | |

उत्तर-पुस्तिका सं.: **Answer Sheet No.:** | | | | | | |

परीक्षार्थी का नाम: **परीक्षार्थी के हस्ताक्षर:**
Name of Candidate: _____; Signature of candidate: _____

परीक्षार्थियों के लिए निर्देश: **Instructions for Candidate:**

कृपया प्रश्न-पुस्तिका, ओएमआर शीट एवं उत्तर–पुस्तिका में दिये गए निर्देशों को ध्यान पूर्वक पढ़ें।	Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.
प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी केवल अंग्रेजी भाषा में ही उत्तर कर सकता है।	Question Paper is in English language. Candidate can answer in English language only.
इस मॉड्यूल/पेपर के **दो भाग** है। **भाग एक** में चार प्रश्न और **भाग दो** में पाँच प्रश्न है।	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions**.**
भाग एक "वैकल्पिक" प्रकार का है जिसके कुल अंक 40 है तथा **भाग दो**, "व्यक्तिपरक" प्रकार है और इसके कुल अंक 60 है।	**PART ONE** is Objective type and carries 40 Marks. **PART TWO** is subjective type and carries 60 Marks.
भाग एक के उत्तर, इस प्रश्न-पत्र के साथ दी गई **ओएमआर उत्तर-पुस्तिका** पर, उसमें दिये गए अनुदेशों के अनुसार ही दिये जाने है। **भाग दो** की उत्तर-पुस्तिका में **भाग एक** के उत्तर **नहीं** दिये जाने चाहिए।	**PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the question paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book for **PART TWO**.
भाग एक के लिए अधिकतम समय सीमा **एक घण्टा** निर्धारित की गई है। **भाग दो** की उत्तर-पुस्तिका, **भाग एक** की उत्तर-पुस्तिका जमा कराने के पश्चात दी जाएगी। तथापि, निर्धारित एक घंटे से पहले **भाग एक** पूरा करने वाले परीक्षार्थी **भाग एक** की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरंत बाद, **भाग दो** की उत्तर-पुस्तिका ले सकते हैं।	Maximum time allotted for **PART ONE** is **ONE HOUR.** Answer book for **PART TWO** will be supplied at the table when the answer sheet for **PART ONE** is returned. However, candidates who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the answer sheet for **PART ONE.**
परीक्षार्थी, उपस्थिति-पत्रिका पर हस्ताक्षर किए बिना अथवा अपनी उत्तर-पुस्तिका, निरीक्षक को सौंपे बिना, परीक्षा हाल नहीं छोड़ सकता हैं। ऐसा नही करने पर, परीक्षार्थी को इस मॉड्यूल/पेपर में अयोग्य घोषित कर दिया जाएगा।	**Candidate cannot leave the examination hall/room without signing on the attendance sheet or handing over his Answer sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.**
प्रश्न-पुस्तिका को खोलने के निर्देश मिलने के पश्चात एवं उत्तर देने से पहले उम्मीदवार यह जाँच कर यह सुनिश्चित कर ले कि प्रश्न-पुस्तिका प्रत्येक दृष्टि से संपूर्ण है।	After receiving the instruction to open the booklet and before answering the questions, the candidate should ensure that the Question booklet is complete in all respect.

जब तक आपसे कहा न जाए तब तक प्रश्न-पुस्तिका न खोलें।

DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.

PART ONE
(Answer all the questions)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

1.1 The decoded instruction is stored in _____.
A) IR
B) PC
C) Registers
D) MDR

1.2 Which registers can interact with the secondary storage?
A) MAR
B) PC
C) IR
D) R0

1.3 In case of, Zero-address instruction method the operands are stored in _____.
A) Registers
B) Accumulators
C) Push down stack
D) Cache

1.4 _____ converts the programs written in Assembly Language into machine instructions.
A) Machine compiler
B) Interpreter
C) Assembler
D) Converter

1.5 The last statement of the source program should be _____.
A) Stop
B) Return
C) OP
D) End

1.6 The minimum time delay between two successive memories read operations is _____.
A) Cycle time
B) Latency
C) Delay
D) None of the above

1.7 _____ is the bottle neck, when it comes to computer performance.
A) Memory access time
B) Memory cycle time
C) Delay
D) Latency

1.8 The logic operations are implemented using _____ circuits.
A) Bridge
B) Logical
C) Combinatorial
D) Gate

1.9 In full adders the sum circuit is implemented using _____.
A) AND & OR gates
B) NAND gates
C) XOR
D) XNOR

1.10 VLSI stands for
A) Very Large Scale Integration
B) Very Large Stand-alone Integration
C) Volatile Layer System Interface
D) None of the above

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

2.1 The PCI bus turns at 33 MHZ and can transfer 32-bits of data (four bytes) every clock tick.
2.2 Cache memories are high-speed buffers which are inserted between the processors and main memory.
2.3 A keyboard has parallel type of asynchronous transfer mode.
2.4 System Call exception is also known as software interrupt.
2.5 Arithmetic operations with fixed point numbers take longer time for execution as compared to with floating point numbers.
2.6 When a word is to be written in an associative memory, address has got to be given.
2.7 Complex Instruction Set Computers (CISC) processors are generally faster than Reduced Instruction Set Computers (RISC) processors.
2.8 Static Dynamic Random Access Memory (SDRAM) is a permanent memory store that required no flow of electricity to be maintained.
2.9 Assembly language is a high level language.
2.10 Address bus is bidirectional.

ROUGH WORK SPACE:

3. Match words and phrases in column X with the closest related meaning/ word(s)/phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

X		Y	
3.1	MIMD stands for	**A.**	Latency ratio
3.2	A binary digit is called a	**B.**	Zero
3.3	A flip-flop is a binary cell capable of storing information of	**C.**	Software
3.4	An address in main memory is called	**D.**	Bit
3.5	The performance of cache memory is frequently measured in terms of a quantity called	**E.**	Logic Operation
3.6	CPU does not perform the operation	**F.**	Physical address
3.7	In Assembly language programming, minimum number of operands required for an instruction is/are	**G.**	uses alphabetic codes in place of binary numbers used in machine language
3.8	Interrupts which are initiated by an instruction are	**H.**	Multiple instruction multiple data
3.9	Assembly language	**I.**	Access time
3.10	The average time required to reach a storage location in memory and obtain its contents is called the	**J.**	One bit
		K.	Local address
		L.	Hit ratio
		M.	Two bit

4. Each statement below has a blank space to fit one of the word(s) or phrase(s) in the list below. Choose the most appropriate option, enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10)

A.	Instruction pointer	**B.**	SISD	**C.**	Code Converter
D.	PC (Program Counter)	**E.**	Primary Storage	**F.**	Instruction register
G.	FFFF	**H.**	Static RAM	**I.**	MIMD
J.	n-bit instruction register	**K.**	Binary micro program	**L.**	90%
M.	87%				

4.1 Logic X-OR operation of (4ACO)H& (B53F)H results _____.

4.2 Virtual memory consists of _____.

4.3 If memory access takes 20 ns with cache and 110 ns without it, then the ratio (cache uses a 10 ns memory) is _____.

4.4 Processors of all computers, whether micro, mini or mainframe must have _____.

4.5 A micro program written as string of 0's and 1's is a _____.

4.6 PC Program Counter is also called _____.

4.7 Von Neumann architecture is _____.

4.8 An n-bit microprocessor has _____.

4.9 The circuit converting binary data into decimal is _____.

4.10 _____ register keeps tracks of the instructions stored in program stored in memory.

ROUGH WORK SPACE:

PART TWO
(Answer any FOUR questions)

5.

a) Differentiate between computer architecture and computer organization.

b) Write a note on:
   i) Interrupt service routine
   ii) RISC vs. CISC computers
   iii) Asynchronous serial transfer
   iv) Memory mapped I/O

(3+[3x4])

6.

a) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic micro-operation to be performed in order to change the value in A to:
   i) 01101101
   ii) 11111101

b) What do you mean by initialization of DMA controller? How DMA Controller works? Explain with suitable block diagram.

(5+10)

7.

a) Convert the following infix expression to reverse polish notation, clearly showing the steps involved.
   A*B+C/D

b) Briefly explain instruction format.

c) Consider a cache with 64 blocks and a block size of 16 bytes. To what block number does byte address 1200 map?

(5+5+5)

8.

a) Derive and explain an algorithm for adding and subtracting two floating point binary numbers.

b) What is Virtual Memory Address Translation? Explain in detail about memory hierarchy with neat diagram.

(8+7)

9.

a) Explain the Working of a Carry-Look Ahead adder.

b) Write an assembly language (8086) program to find the largest number from the list of ten numbers defined as word at NUM. Put the result at LAR, which is defined as word.

(8+7)

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ROUGH WORK SPACE:

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