C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What is the difference between serial and parallel transfer?

b) What is the difference between a direct and indirect address instruction in terms of number of memory references made to bring and operand into a processor register?

c) What are the two instructions needed in the basic computer in order to set the *E* flip-flop to 1?

d) Define microinstruction.

e) Explain the difference between spatial and temporal locality.

f) List various cache mapping schemes. Explain any one in detail.

g) How many switch points are there in a crossbar switch network that connects *p* processors to *m* memory modules?

(7x4)

2.

a) For each radix-*r* determine the largest number *max* that is representable with the indicated *k* number of digits and the minimum number of digits (say K) required to represent all natural numbers less then equal to 999999.

i) $r = 2, k = 16$

ii) $r = 10, k = 8$

iii) $r = 8, k = 6$

b) Prove that the multiplication of two *n*-digit numbers in base *r* gives a product no more than 2*n* digits in length. Show the step-by-step multiplication process using Booth algorithm for (+15) × (-13) assuming 5-bit registers are holding the signed numbers.

(9+9)

3.

a) Write a program in assembly language to evaluate the expression X = (A * (B + C * (D + E))) / (F * (G + H)

i) Using a general register computer with three address instructions.

ii) Using an accumulator type computer with one address instruction.

b) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of the seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word.

c) What are basic differences between a branch instruction, a call subroutine instruction, and program interrupt?

(6+6+6)

4.

a) Starting from an initial value of *R* = 11011101, determine the sequence of binary values in *R* after a logical shift-left, followed by a circular shift-right, followed by logical shift-right, followed by a circular shift-left.

b) The 8-bit registers AR, BR, CR and DR initially have the following values

AR = 11110010

BR = 11111111

CR = 10111001

DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

$AR \leftarrow AR + BR$	Add BR to AR
$CR \leftarrow CR \wedge DR,\ BR \leftarrow BR + 1$	AND DR to CR increment BR
$AR \leftarrow AR - CR$	Subtract CR from AR

c) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.
   i) How many selection inputs are there in each multiplexer?
   ii) What sizes of multiplexers are needed?
   iii) How many multiplexers are there in the bus?

(6+6+6)

5.

a) What is cache coherence, and why is it important in shared-memory multiprocessors systems? How can the problem be resolved with a snoopy cache controller?

b) Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment.

c) Consider a computer with four floating-point pipeline processors. Suppose that each processor uses a cycle time of 40ns. How long will it take to perform 400 floating-point operations? Is there a difference if the same 400 operations are carried out using a single processor with a cycle time of 10ns?

(6+6+6)

6.

a) What is the difference between isolated I/O and memory-mapped I/O? What are the advantages and disadvantages of each?

b) How many characters per second can be transmitted over a 1200-baud line in each of the following mode? (Assume a character code of 8 bits).
   i) Synchronous serial transmission
   ii) Asynchronous serial transmission with two stop bits.
   iii) Asynchronous serial transmission with one stop bit.

c) A DMA controller transfers 16-bit words to memory using cycle stealing. The words are assembled from a device that transmits characters at a rate of 2400 characters per second. The CPU is fetching and executing instructions at an average rate of one million instructions per second. By how much will the CPU be slowed down because of the DMA transfer?

(6+6+6)

7.

a) A computer system has a 1 GB main memory. It also has a 4K-byte cache organized as a 4-way set associative, with 4 blocks per set and 64 bytes per block. Calculate the number of bits in the Tag, Set index, and Byte offset fields of the memory address format.

b) The access time of a cache memory is 100 ns and that of main memory is 1000 ns. It is estimated that 80% of the memory requests are read and remaining 20% for write. This hit ratio for read access only is 0.9. A write through procedure is used.
   i) What is the average access time of the system considering only memory read cycles?
   ii) What is the average access time of the system for both read and write requests?
   iii) What is the hit ratio taking into consideration the write cycles?

c) The logical address space in a computer system consists of 128 segments. Each segment can have up to 32 pages of 4K words in each. Physical memory consists of 4K blocks of 4K words in each. Formulate the logical and physical address formats.

(6+6+6)