A4/B1.4-R4 : COMPUTER SYSTEM ARCHITECTURE

अवधि : 03 घंटे **अधिकतम अंक : 100**
DURATION : 03 Hours **MAXIMUM MARKS : 100**

ओएमआर शीट सं. : **OMR Sheet No. :**						

रोल नं. : **Roll No. :** | | | | | | |

उत्तर-पुस्तिका सं. : **Answer Sheet No. :**						

परीक्षार्थी का नाम : **परीक्षार्थी के हस्ताक्षर :**
Name of Candidate : _____; **Signature of Candidate :** _____

परीक्षार्थियों के लिए निर्देश :	**Instructions for Candidate :**
कृपया प्रश्न-पुस्तिका, ओएमआर शीट एवं उत्तर-पुस्तिका में दिये गए निर्देशों को ध्यानपूर्वक पढ़ें।	Carefully read the instructions given on Question Paper, OMR Sheet and Answer Sheet.
प्रश्न-पुस्तिका की भाषा अंग्रेजी है। परीक्षार्थी केवल अंग्रेजी भाषा में ही उत्तर दे सकते हैं।	Question Paper is in English language. Candidate can answer in English language only.
इस मॉड्यूल/पेपर के **दो भाग** हैं। **भाग एक** में **चार** प्रश्न और **भाग दो** में **पाँच** प्रश्न हैं।	There are **TWO PARTS** in this Module/Paper. **PART ONE** contains **FOUR** questions and **PART TWO** contains **FIVE** questions.
भाग एक ''वैकल्पिक'' प्रकार का है जिसके कुल अंक 40 है तथा **भाग दो** ''व्यक्तिपरक'' प्रकार है और इसके कुल अंक 60 है।	**PART ONE** is Objective type and carries 40 Marks. **PART TWO** is Subjective type and carries 60 Marks.
भाग एक के उत्तर, इस प्रश्न-पत्र के साथ दी गई **ओएमआर उत्तर-पुस्तिका** पर, उसमें दिये गए अनुदेशों के अनुसार ही दिये जाने हैं। **भाग दो** की उत्तर-पुस्तिका में **भाग एक** के उत्तर **नहीं** दिये जाने चाहिए।	**PART ONE** is to be answered in the **OMR ANSWER SHEET** only, supplied with the Question Paper, as per the instructions contained therein. **PART ONE** is **NOT** to be answered in the answer book for **PART TWO**.
भाग एक के लिए अधिकतम समय सीमा **एक घण्टा** निर्धारित की गई है। **भाग दो** की उत्तर-पुस्तिका, **भाग एक** की उत्तर-पुस्तिका जमा कराने के पश्चात् दी जाएगी। तथापि, निर्धारित एक घंटे से पहले **भाग एक** पूरा करने वाले परीक्षार्थी **भाग एक** की उत्तर-पुस्तिका निरीक्षक को सौंपने के तुरंत बाद, **भाग दो** की उत्तर-पुस्तिका ले सकते हैं।	Maximum time allotted for **PART ONE** is **ONE HOUR**. Answer book for **PART TWO** will be supplied at the table when the Answer Sheet for **PART ONE** is returned. However, candidates who complete **PART ONE** earlier than one hour, can collect the answer book for **PART TWO** immediately after handing over the Answer Sheet for **PART ONE** to the Invigilator.
परीक्षार्थी, उपस्थिति-पत्रिका पर हस्ताक्षर किए बिना एवं अपनी उत्तर-पुस्तिका, निरीक्षक को सौंपे बिना, परीक्षा हॉल/कमरा नहीं छोड़ सकता है। ऐसा नहीं करने पर, परीक्षार्थी को इस मॉड्यूल/पेपर में अयोग्य घोषित कर दिया जाएगा।	**Candidate cannot leave the examination hall/room without signing on the attendance sheet and handing over his/her Answer Sheet to the invigilator. Failing in doing so, will amount to disqualification of Candidate in this Module/Paper.**
प्रश्न-पुस्तिका को खोलने के निर्देश मिलने के पश्चात् एवं उत्तर लिखना आरम्भ करने से पहले उम्मीदवार यह जाँच कर यह सुनिश्चित कर लें कि प्रश्न-पुस्तिका प्रत्येक दृष्टि से संपूर्ण है।	After receiving the instruction to open the booklet and before starting to answer the questions, the candidate should ensure that the Question Booklet is complete in all respect.

जब तक आपसे कहा न जाए, तब तक प्रश्न-पुस्तिका न खोलें।
DO NOT OPEN THE QUESTION BOOKLET UNTIL YOU ARE TOLD TO DO SO.

PART ONE

(Answer all the questions.)

1. Each question below gives a multiple choice of answers. Choose the most appropriate one and enter in the "OMR" answer sheet supplied with the question paper, following instructions therein. **(1x10=10)**

1.1 Which of the following is concerned with the way the hardware component operate and the way they are connected together to form the computer system ?

(A) Computer organization

(B) Computer design

(C) Computer architecture

(D) Computer system

1.2 Which of the following devices contain thousands of gates within a single package ?

(A) Small-scale integration

(B) Medium-scale integration

(C) Large-scale integration

(D) Very large-scale integration

1.3 Which of the following is equivalent octal representation of 110111001101 binary ?

(A) 6715

(B) DCD

(C) 131213

(D) 5167

1.4 Which of the following register holds an address for the memory unit ?

(A) MBR

(B) MAR

(C) IR

(D) PC

1.5 In which of the following the bits in second part of the instruction designate the address of a memory word in which the address of operand found ?

(A) Actual operand

(B) Indirect address

(C) Direct address

(D) Immediate address

1.6 A memory-reference instruction has an address part of :

(A) 12 bits

(B) 10 bits

(C) 8 bits

(D) 6 bits

1.7 CLA (Clear Accumulator) is an example of :

(A) Direct address MRI

(B) Indirect address MRI

(C) Non-MRI

(D) Pseudo instruction

1.8 Which of the following notation places the operator after the operands ?

(A) Postfix

(B) Prefix

(C) Infix

(D) None of the above

1.9 Which of the following instruction is an example of single accumulator organization ?

(A) ADD R1, R2, R3

(B) ADD X

(C) PUSH X

(D) MOV R1, R2

1.10 Which of the following bus from the processor is attached to all peripherals ?

(A) I/O Bus

(B) Data Bus

(C) Address Bus

(D) Control Bus

2. Each statement below is either TRUE or FALSE. Choose the most appropriate one and enter your choice in the "OMR" answer sheet supplied with the question paper, following instructions therein. **(1x10=10)**

2.1 The input-output relationship of the binary variables for each gate can be represented in tabular form by truth-table.

2.2 Half-adder is a combinational circuit that form the arithmetic sum of three inputs.

2.3 Multiplexer may have an enable input to control the operation of the unit.

2.4 1110011 is equivalent binary 2's complement representation of -14.

2.5 A bus system can be constructed with three-state gates instead of multiplexer.

2.6 Computers that have a single-processor register in that usually operation is performed with memory operand and the content of accumulator (AC).

2.7 In the hardwired control organization, the control information is stored in control memory.

2.8 When IEN (Interrupt Enable) is cleared to 0, the flags cannot interrupt the computer.

2.9 For arithmetic shift-left it is necessary that the added bit in the least significant position be 0.

2.10 A status command is issued to activate the peripheral and to inform it what to do.

SPACE FOR ROUGH WORK

3. Match words and phrases in column X with the closest related meaning / word(s) / phrase(s) in column Y. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10=10)

X		Y	
3.1	Binary information is represented in digital computers by physical quantities called	**A.**	an overflow.
3.2	The simplest possible shift register is one that uses only	**B.**	register transfer.
3.3	A memory stores binary information in a group of bits called	**C.**	a zero-address instruction.
3.4	When two unsigned numbers are added, an overflow is detected from the end carry out of	**D.**	interrupt.
3.5	Control signals determine which register is selected by the bus during each particular	**E.**	MRI-instruction.
3.6	The ALU performs an operation and the result of the operation is then transferred to	**F.**	words.
3.7	Only three bits of the instruction are used for the operation code.	**G.**	pseudo instructions.
3.8	The symbols ORG, DEC and END are called	**H.**	Accumulator.
3.9	A skip instruction does not need an address field and is therefore	**I.**	the most significant bit.
3.10	A division operation may result in a quotient with	**J.**	signals.
		K.	the sign bit.
		L.	destination register.
		M.	flip-flop.

4. Each statement below has a blank space to fit one of the word(s) or phrases in the list below. Enter your selection in the "OMR" answer sheet supplied with the question paper, following instructions therein. (1x10=10)

A.	decoder	**B.**	SKI instructions	**C.**	Stack
D.	ALU	**E.**	instruction code	**F.**	Circular shift
G.	Interrupt	**H.**	Boolean function	**I.**	assembler
J.	adder	**K.**	register	**L.**	subtraction operation
M.	bus				

4.1 A(n) _____ can be transformed from an algebraic expression into a logic diagram composed of AND, OR and inverter gates.

4.2 A(n) _____ is a combinational circuit that converts binary information from the n coded inputs to a maximum of 2n unique output.

4.3 Complements are used in digital computers for simplifying the _____ and for logical manipulation.

4.4 The selective-set operation sets to 1 the bits in _____.

4.5 _____ is accomplished by connecting the serial output of shift register to its serial output.

4.6 A(n) _____ is group of bits that instruct the computer to perform a specific operation.

4.7 The translation of a symbolic program into a binary is done by a special program called a(n) _____.

4.8 The _____ checks the input flag to see if a character is available for transfer.

4.9 A(n) _____ is a storage device that stores information in such a manner that the item stored last is the first item retrieved.

4.10 The _____ are used for routing data and arranging the printed text into a prescribed format.

PART TWO

(Answer any FOUR questions.)

5. (a) What is 2's complement representation perform the subtraction for the following operation :

$(+42)+(-13)$ and $(-42)-(-13)$

(b) Show the block diagram of the hardware that implements the following register transfer statement:

yT2 : R2←R1, R1←R2

(c) The following memory units are specified by the number of words times the number of bits per word. How many address lines and input-output data line are needed in each case ?

(i) $2K \times 8$

(ii) $32K \times 8$

(iii) $16M \times 16$

(iv) $8G \times 16$

(5+6+4=15)

6. (a) What is the difference between a direct and indirect address instruction ? How many references to memory are needed for each type of instruction to bring an operand into a processor register ?

(b) What is meant by Page replacement ? Explain any 3 page replacement algorithms in detail.

(c) What are the differences between a branch instruction, a call subroutine instruction and a program interrupt ? Give the examples of external interrupts and internal interrupts.

(5+5+5=15)

7. (a) With the help of diagram discuss the working of DMA.

(b) Convert the following numerical arithmetic expression into reverse polish notation and show the stack operations for evaluating the numerical results.

$(3+4)\ [10\ (2+6)+8]$

(7+8=15)

8. (a) Show the step-by-step multiplication process for $(+15)\times(-13)$ using Booth's algorithm when the following binary numbers are multiplied. Assume 5-bit register that hold signed numbers. The multiplicand in is $+15$.

(b) List four peripheral devices that produce an acceptable output for a person to understand. What is the difference between isolated I/O and memory mapped I/O ? What are the advantages and disadvantages of each ?

(7+8=15)

9. (a) Show the contents of register A, B, Q and SC during the decimal division of 1680/32. Assume two-digit register.

(b) What do you understand by level of memory hierarchy ? Explain each of these levels in detail ?

(c) Differentiate Cache and RAM.

(7+5+3=15)

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