C0-R4.B4: COMPUTER SYSTEM ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Starting from an initial value of R = 11010111, determine the sequence of binary values of R after a logical shift left, followed by a circular shift-right, followed by a logical shift right and a circular shift right.

b) Perform the arithmetic operations (+42) + (-13) and (-42) – (-13) in binary using signed-2's complement representation for negative numbers.

c) Design a 4-bit combinational circuit decrementer using 4 full-adder circuits..

d) Convert the following infix expression to postfix expression, clearly showing the steps involved.

5 * (((9 + 8) + (4 * 6)) - 7)

e) What is Interrupt Service Routine?

f) Differentiate between Serial and Parallel Ports.

g) Differentiate between Programmed Driven I/O and Memory Mapped I/O.

(7x4)

2.

a) What is the difference between a direct and an indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand into a processor register?

b) The content of *AC* in the basic computer is hexadecimal A937 and the initial value of *E* is 1. Determine the contents of *AC, E, PC, AR*, and *IR* in hexadecimal after the execution of the CLA instruction. Repeat 11 more times starting from each one of the register-reference instructions. The initial value of *PC* is hexadecimal 021.

c) Suppose the control memory has 4096 words of 24 bits each. Answer the following:

i) How many bits are there in the control address register?

ii) How many bits are there in each of the four inputs shown going into the multiplexers?

iii) What are the number of inputs in each multiplexer and how many multiplexers are needed?

(6+6+6)

3.

a) An 8-bit register contains the binary value 10011100. What is the register value after arithmetic shift right? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow.

b) The content of *PC* in the basic computer is 3AF (all numbers are in hexadecimal). The content of *AC* is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F.

i) What is the instruction that will be fetched and executed next?

ii) Show the binary operation that will be performed in the *AC* when the instruction is executed.

iii) Give the contents of registers *PC, AR, DR, AC, and IR* in hexadecimal and the values of *E, I,* and the sequence counter *SC* in binary at the end of the instruction cycle.

(6+12)

4.

a) You have an L1 data cache, L2 cache, and main memory. The hit rates and hit times for each are: 50% hit rate, 2 cycle hit time to L1. 70% hit rate, 15 cycle hit time to L2. 100% hit rate, 200 cycle hit time to main memory. What fractions of accesses are serviced from L2? From main memory? What is the miss rate and miss time for the L2 cache?

b) What do you understand by Cache Coherence? What is the Cache Coherence problem in shared memory multiprocessors? Discuss briefly of its solutions.

(9+9)

5.

a) Explain the Working of a parallel Adder/ Subtractor Circuit.

b) Write an assembly language (8086) program to find the multiplication to two 8 bit numbers in Assembly Language.

(9+9)

6.

a) Explain both multiplication algorithms to multiply two binary integers along with the hardware implementation.

b) Explain the Working of a Ripple Adder Circuit.

(9+9)

7.

a) Explain in detail about Virtual Memory Address Translation?

b) What are the virtual memory parameters that are required to be set by the system designer?

c) Explain how a virtual address can be converted into a physical address?

(6+6+6)