National Institute of Electronics & Information Technology

<table>
<tr><th colspan="4">Advt. No. NHQ12/22/2025-NC (3160304)
Document Verification and Interview Schedule for Edtech Project</th></tr>
<tr><th>Date</th><th>Subject</th><th colspan="2">Schedule</th></tr>
<tr><td rowspan="2">11th September 2025
(Thursday)</td><td rowspan="2">Team Lead (VLSI Design),
VLSI Design Expert/ Jr. VLSI Engineer,
Sr. Trainers (VLSI Design)/ Sr. VLSI Engineer,
Team Leader (platform Development Team),
DevOps Engineer</td><td>Document Verification</td><td>9:30 AM - 12:00 PM</td></tr>
<tr><td>Interview</td><td>11:00 AM onwards</td></tr>
<tr><td rowspan="2">12th September 2025
(Friday)</td><td rowspan="2">Full Stack Engineer,
Graphics Designer,
Sr. Resource Person,
Consultant (Design Verification & EDA Integration)</td><td>Document Verification</td><td>9:30 AM - 12:00 PM</td></tr>
<tr><td>Interview</td><td>11:00 AM onwards</td></tr>
<tr><td colspan="4">NOTE: List of Eligible Candidates will be uploaded in due course.</td></tr>
<tr><td colspan="4">Venue for Document Verification and Interview:
National Institute of Electronics & Information Technology
NIELIT Bhawan, Plot No. 3, PSP Pocket,
Sector-8, Dwarka, New Delhi-110077</td></tr>
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