Last date for Submission: 31st July 2017

Expression of Interest (EOI)

For conduct of
All India PG Diploma Program
from
AICTE approved Institutions and Deemed Universities

NIELIT Calicut

A Centre of NIELIT, New Delhi
An Autonomous Scientific Society of Ministry of Electronics and Information Technology (MeitY),
Government of India

P.B. No. 5, NIT Campus Post, Calicut 673601 Kerala
Phone: (0495) 2287266, Fax: (0495) 2287168
Web:http://nielit.gov.in/calicut/

Contents

EXPRESSION OF INTEREST

1.0 Introduction

NIELIT Calicut, a Centre of NIELIT, New Delhi, an Autonomous Scientific Society of Ministry of Electronics and Information Technology, Government of India is engaged in education, training and consultancy services in advanced areas of IECT and/or intended to extend quality education to masses through various schemes and programs.

All India PG Diploma Programs of NIELIT are intended to provide value addition to engineering students with focus on practical training and providing knowledge in recent trends of industry requirements. The students on successful completion of these programs can be directly employed by the industries on job, thus increases the employment opportunity.

NIELIT Calicut is interested in partnering with AICTE approved institutions and deemed universities for the implementation of the following programs.

1. VLSI & Embedded Hardware Design
2. Embedded Real time Systems
3. ASIC Design and Verification

2.0 Objectives

The broad objectives/aims are:

- To design, develop and conduct value addition programs in-line with the requirement of Industry.
- To generate quality manpower in-line with the ESDM Policy of Govt. of India
- Provide practical skill and knowledge to bridge the gap between academia and industry
- Developing and implementing content as per the industry requirement to enhance the knowledge in related areas and increase immediate employment opportunities.

3.0 Invitation for EoI

3.1 NIELIT Calicut invites Expression of Interest (EoI) from AICTE approved institutions and deemed universities to conduct All India PG Diploma Program and provide facilities as per the requirement of funding agency and NIELIT.

3.2 Interested applicants may download the format and other documents related to EoI from the website http://nielit.gov.in/calicut

3.3 Interested applicants at the time of submission of response to the EoI, should submit **non- refundable demand draft of Rs. 1,000/- (Rupees one thousand only) in-favor of "Executive Director NIELIT Calicut" payable at Calicut**. Failure to do so will result in rejection of the EoI. (**Institutions run by the Government (State & Central) are exempted from the above fee)**

3.4 The Expression of Interest must be delivered to the below address by 17.00 hrs on 31st July 2017

The Executive Director
NIELIT Calicut
Post Box No. 5
NIT Campus P O
Calicut 673601
Kerala

Contact details:
Email: purchase@calicut.nielit.in
Phone: 0495 2287179/2287266.

4.0 Scope of Work

4.1 The applicant would be required to study the objectives of the proposed training programs and its deliverables. The broad areas of scope of work includes, joint identification of trainees, registration, imparting training, career guidance and placement support. The areas of training
4.2 Duration and related information are given in Annexure II A, IIB, IIC.
4.3 Provide / create required infrastructure and conduct the training program as per the course requirement & schedule decided
4.4 The selected / empanelled organization shall be considered for conducting the training initially for two years which may be extended depending on performance/requirement for the second and subsequent phase of training.
4.5 The training has to be conducted as per the modalities of the MoU given under Annexure I

5.0 Eligibility Criteria

5.1 **Only** AICTE approved institutions and deemed universities are eligible to apply

6.0 Criteria for Empanelment

6.1 Interested institutions should submit a letter of interest along with their infrastructure details in the specified format as given in Annexure II &IV.
6.2 The information provided should be sufficient such that the infrastructure and other requirements are fulfilled as per the requirement to carry out the training.
6.3 The selection/empanelment will be in accordance with the criteria set by NIELIT and based on the evaluation by the committee constituted for the purpose.

6.4 The short-listed/empanelled institutions will be communicated and on agreeing the terms shall be invited become an accredited Center of NIELIT / enter into an agreement with NIELIT Calicut.

6.5 NIELIT Calicut will have the right to reject any or all EoIs, received in response to this invitation and its decision in this regard shall be final and binding.

7.0 **Procedure for submission**

7.1 Download the detailed information along with application format available in our website http://nielit.gov.in/calicut

7.2 Covering letter along with information of contact person should be made strictly as per the format given in Annexure III

7.3 Provide information on infrastructure and other relevant information only in the format provided as Annexure- IV. Information submitted in other formats/ in complete applications will be rejected.

7.4 Attach documentary proof where ever required in support of your claim.

7.5 Add as attachment additional information, if any.

7.6 Attach demand draft for Rs.1000/- drawn in-favor of "Executive Director NIELIT Calicut" payable at Calicut.

8.0 **Guidelines for submission of EoI**

8.1 Agency must enclose a covering letter on Agency's Letter Head while sending the application- Annexure III

8.2 The EOIs must be sent in sealed cover so as to reach NIELIT Calicut within the stipulated time. The EOIs will be evaluated strictly as per laid down criteria. Therefore, before sending the EOIs, the bidder agency must satisfy that they fulfill all the eligibility criteria. The related proof of experience, details of office set-up etc., as asked for, must be enclosed/detailed out for evaluating the EOIs.

8.3 Thedetails must be furnished as per formats enclosed in this document and strictly as per serial order. The information intended to be supplied should be furnished in such a manner that the same satisfies the need/requirement of EOI under various heads and is self-explanatory.

8.4 In case desired documents/proofs are not enclosed, the EOI shall be rejected and no clarification/enquiry will be sought/made.

8.5 The last date of receiving the EOIs shall be adhered strictly. EOIs received after the last date will not be considered and no further action will be taken on such EOIs. However, if the last date is declared as holiday, the next working day on which office is opened will be treated as the last date of receiving the EOIs. The EOIs should be physically received in this office at NIELIT Calicut Center.

8.6 The envelopes should be super scribed with "**EoI from AICTE approved institutions and deemed universities to conduct All India PG Diploma".**

9.0 **Validity of EoI submitted**

The EoI submitted by the applicant shall remain valid for a period of 60 days after the closing date (deadline) for submission of EoI prescribed in this document. EoI valid for shorter period may be rejected as non-responsive. NIELIT Calicut may solicit the applicants' consent to an extension of EoI validity (but without the modification in their EoI).

10.0 Disclaimer

10.1 The information submitted in response to this EoI may be subject to public release (as per RTI norms). Therefore, do not include proprietary or confidential business information in your response. Applicants responding to this invitation assume the risk of public disclosure if confidential information is included.

10.2 This invitation is for information purposes only and does not constitute a solicitation or Request for Proposal (RFP). This notice is not to be construed as a commitment by the NIELIT to contract for services. Please be advised that NIELIT Calicut will not pay for any information provided as a result of this invitation and will not recognize or reimburse any cost associated with any EoI submission.

10.3 This EoI does not entail any commitment on the part of NIELIT Calicut, either financial or otherwise.

10.4 NIELIT Calicut reserves the right to accept or reject any or all EoI without incurring any obligation to inform the affected applicant/s of the reasons.

10.5 NIELIT Calicut empanelment as Training Institute does not create any obligation on the part of NIELIT Calicut in terms of providing business or in any other area.

10.6 At any time prior to deadline for submission of EoIs, NIELIT Calicut may for any reason, modify the EoI document. The amendment document shall be notified through website and such amendments shall be binding on them

Annexure I

MEMORANDUM OF UNDERSTANDING (MoU)
Between
National Institute of Electronics and Information Technology, Calicut
and
XXX University

PREAMBLE

National Institute of Electronics and Information Technology (NIELIT) is engaged in education, training and consultancy services in advanced areas of IECT and/or intended to extend quality education to masses through various schemes and programs.

All India PG Diploma Programs of NIELIT is intended to provide value addition to engineering students with focus on practical training as providing knowledge in recent trends of industry requirements. The students on successful completion of these programs can be directly employed by the industries on job, thus increases the employment opportunity.

The broad objectives/aims are:

- To design, develop and conduct value addition programs in-line with the requirement of Industry.
- To generate quality manpower in-line with the ESDM Policy of Govt. of India
- Provide practical skill and knowledge to bridge the gap between academia and industry
- Developing and implementing content as per the industry requirement to enhance the knowledge in related areas and increase immediate employment opportunities.

1.0 The MoU

1.1 This MoU entered into this _____day of _____ Two Thousand and ___ (2017) by and between NIELIT CALICUT, A unit of NIELIT NEW DELHI, An autonomous body of Ministry of Electronics and Information Technology, Government of India, registered under Societies' Registration Act 1860 having its Head office at Electronics Niketan, 6, CGO Complex, New Delhi-110003, and the Calicut Centre located at Chathamangalam, NIT Campus post, Calicut 673 601 (Kerala) (hereinafter called "NIELIT CALICUT" which expression shall where the context so admits include its successors and permitted assignees) of the first part,

AND

1.2 XXX University, located at XXXXX, XXXX (hereinafter called "XXX" which expression shall where the context so admits include its successors and permitted assignees) of the second part

Whereas the XXX University party of the second part has approached the party of first part and requested for conducting the said program for the benefit of their students in their college premises.

Whereas the party of the first part has agreed to party of second part on such terms and conditions mutually agreed and together arrived into an Understanding as follows

2.0 SCOPE OF MOU

2.1 This MOU broadly defines the mode and methodology of conducting training programme in the following All India PG Diploma Programmes i)VLSI & Embedded Hardware Design, ii)Embedded Real time Systems, and iii)ASIC Design and Verification and spells out the rights and responsibilities of the parties hereto.

3.0 RESPONSIBILITIES OF PARTIES

3.1 Responsibilities of NIELIT CALICUT.

1. Provide XXXX with the curriculum, Lab notes and workbook of the courses.
2. Preparation of laboratory requirements (Hardware and Software).
3. Provide the centre with a training calendar for conducting the courses.
4. Assuring the quality of the training courses offered by XXX by conducting audits periodically and inspection of the training facilities at XXX as and when felt necessary.
5. Provide a hardcopy of the course source book which would be the reference point with regards to the various requirements to be met by XXX U for conduct of the all India PG Diploma Programmes i) VLSI & Embedded Hardware Design, ii)Embedded Real time Systems, and iii)ASIC Design and Verification.
6. Provide Faculty orientation programs to the technical members of the XXX U on the need basis at NIELIT, Calicut on a chargeable basis. The cost of faculty training program will be worked based on the prevailing man hour rates and infrastructure charges
7. Technical support in establishing the lab setup at XXX U.
8. Allow access to attend video lectures on selected topics related to the course as and when telecast.

3.2 Responsibilities of XXX U.

1. Should strictly follow the source book to conduct the Post Graduate Diploma Programmes in i) VLSI & Embedded Hardware Design, ii)Embedded Real time Systems, and iii)ASIC Design and Verification
2. Establish, provide and upgrade complete infrastructure as recommended by NIELIT CALICUT for the conduction of the said PG diploma programs at XXX U.
3. Conduct theory and practical sessions and provide course material to the students as prescribed in the source book
4. XXX U shall mobilise and select the students for the courses as per the eligibility criteriaand ensure that they have completed graduation for the award of PG Diploma.
5. Recruit and Select qualified Faculty to conduct the courses and the remuneration for faculty shall be made by XXX U.
6. Provide active placement support to the students of XXX U.
7. Procure/Purchase/obtain license of software/hardware and install/maintain/upgrade specified software in all machines for lab setups, as specified in the source book.
8. Ensure that the training programmes are executed at a very high degree of quality.
9. Identify and nominate program coordinator to conduct the courses at XXX U and interface with NIELIT CALICUT, so as to plan, implement, monitor and review the training programme.
10. Shall provide / distribute the course material in Hard or Soft copy to the

registered students on the day of commencement of the course.

11. Maintain Course and Student records like course schedule, Students' identification details, attendance, progress of the student, successful completion, issue of certificates, details and reasons of discontinuing students etc.,
12. Shall provide the list of registered students before starting of the batch to NIELIT Calicut and the 30% share of NIELIT, Calicut should be remitted within one month of start of the course.

4.0 FINANCIAL ASPECTS

4.1 NIELIT CALICUT, Calicut and XXX U, shall share the course fee collected from the participants in the ratio of 30:70 respectively. XXX U shall pay the service tax on the total course fee and 30% of the course fee shall be paid to NIELIT Calicut. NIELIT Calicut reserves the rights to revise the fees as and when required.

4.2 The general guidelines on fees to be charged from the students is given in annexure the same shall be valid for one year. However XXX U will have the right to subsidize at their own cost the training fee as per market conditions.

4.3 XXX U Guarantees to NIELIT CALICUT that, during the initial period of 12 months, NIELIT will be paid its share for a minimum number of **25** enrollments for each of the programmes, such minimum guaranteed enrolments for the subsequent years will be decided mutually at the beginning of the year. However, in case the actual number of enrolments is more than the minimum, NIELIT CALICUT will be paid as per actual enrolments

4.4 XXX U shall collect the fees from the students. Payment of NIELIT CALICUT's share in respect of training programs shall be made within one (01) month (30 days) by way of

a) Demand Draft from any Nationalised Bank in favour of "Director, NIELIT, Calicut" payable at Calicut (Kerala). Or

b) By Direct Deposit/Online Transfer to our SBI SB A/c No 10401158037 (IFSC: SBIN0002207) under intimation of details of payment like UTR/Journal ID, date, purpose and details of transfer etc to us.

c) By using the facility SBI-Collect under intimation of SBI-Collect Reference Number and purpose and details of the transfer to us.

d) Possibility of opening an escrow account shall be discussed and finalised on signing the MoU.

XXX U agrees to pay a penalty at 18% per annum prorated to number of days of delay in submitting the share of NIELIT CALICUT after the one month (30 days) period of the commencement of the course. (In any case the delay should not exceed more than 6o days)

4.5 XXX U agrees to provide to NIELIT CALICUT a security deposit by means of a bank guarantee/fixed deposit valid for 18 months from the date of agreement and renewable after the above period to the tune of the amount (equal to NIELIT share on fee of 25 students proportional to the programs identified) XXX is liable to pay NIELIT CALICUT for the minimum number of students as mentioned at para 4.3 above.

4.6 The party XXX U shall have the complete responsibility in managing the administrative, publicity and financial matters also providing infrastructure facilities, carry out the admission formalities, collection of fee, maintaining

discipline and attending administrative matters with regards to smooth conduct of courses, administrative correspondence, and financial transactions and prevent any deficiency in service relating to implementation of matters in MOU. The NIELIT shall have no responsibility to any third party in this regard.

5.0 COMMUNICATION

5.1 Any communication or notice or intimation shall be addressed to the Nodal contacts of the respective parties and sent to their registered address of the parties concerned and such a communication sent by e-mail, tele-fax, registered air-mail shall be deemed to be sufficient provided such communication, notice or intimation shall be issued reasonably early before any action is done relating to that.

6.0 CONFIDENTIALITY and NON-DISCLOSURE

6.1 Any software/hardware material, product specifications, designs, financials, information, documents shall be deemed to be in private domain and it shall not be made public or shared with any other party without the prior written consent of the party which owns it.

6.2 The material shall be treated as confidential for a minimum period of two years after this MOU comes to an end or as mutually agreed from time to time.

7.0 INFRASTRUCTURE AND OTHER FACILITIES

7.1 The norms and guidelines for providing infrastructure and other facilities stipulated by NIELIT CALICUT, related to the courses from time to time shall be binding on XXX U.

7.2 NIELIT CALICUT shall have the exclusive rights to inspect the laboratory facilities, records maintained, class schedules etc., of the institute at any point during the working hours of the institute and make suggestions to improve the facilities.

8.0 ADVERTISEMENT AND PUBLICITY

8.1 XXX U may undertake the marketing and promotional campaigns of the courses by advertising in the newspapers or by way of conducting seminars at the engineering colleges, etc about the courses with the permission of NIELIT CALICUT.

9.0 EVALUATION, EXAMINATION AND CERTIFICATION SYSTEM

9.1 NIELIT CALICUT shall be responsible for conduct and evaluation of module end theory examinations through on line/ pen and paper examinations. The module end practical exam shall be conducted with the help of subject experts deputed for the purpose by NIELIT or through experts from NIELIT administering the exam through remote login. XXX U has to provide the necessary facilities, equipment, software, support staff and connectivity free of cost for the conduct of the examination.

9.2 The statement of marks and final diploma certificate will be issued by NIELIT CALICUT. The marks memo shall be prepared by XXX U and signed by the Program Coordinator and forwarded to NIELIT CALICUT for the signature of Program Coordinator, NIELIT CALICUT. The Diploma Certificates will be prepared by XXX U, signed by The Chairman, XXX U and forwarded to NIELIT CALICUT for the signature of The

Director, NIELIT CALICUT.

9.3 XXX U, on its own will not conduct the same or similar course without prior permission of NIELIT CALICUT.

10.0 INTELLECTUAL PROPERTY

10.1 It is expressly stated by the Party of the First Part, and agreed by the party of the second Part, that all the intellectual property rights, to and in the course content, course name, syllabus, methodology, assignments, question papers, website content, etc. are the exclusive intellectual property of NIELIT CALICUT, Calicut and that XXX U shall without permission not: -

(a) Reproduce in any form, make any modifications, alterations therein or deletions thereto.

(b) Make any copies, permit to publish or cause to be published the said as its own.

11.0 VALIDITY OF THE AGREEMENT

11.1 This agreement shall be valid for a period of two years from the date of formal signature by both parties. This agreement may be renewed / extended as may be mutually agreed upon by both the parties.

12.0 FORCE MAJEURE

12.1 Neither party shall be held responsible for non-fulfilment of their respective obligations under this agreement due to the exigency of one or more of the events such as but not limited to acts of God, war, flood earthquakes, strike, lockouts epidemics, riots, civil commotion, etc. provided on the occurrenceand cessation of any such events, the party affected thereby shall give a notice in writing to the other party within one month of such occurrence or cessation. If the force-majeure conditions continue beyond six months, the parties shall then mutually decide about the future course of action.

13.0 During the operation of this MOU in force and two years after expiry of the MOU, XXX U, on its own will not start any new such programs having same title and structure.

14.0 ARBITRATION

14.1 In the event of any dispute or difference between the parties hereto, such disputes or differences shall be resolved amicably by mutual consultations. If such resolution is not possible, then, the unresolved dispute or difference shall be settled by arbitration with the rules of arbitration of the Indian council of arbitration at Calicut. The award of the Arbitrator shall be binding upon parties to the dispute. All discussions / meetings for dispute resolutions will take place at Calicut.

14.2 All disputes arising between the parties to this MoU shall be subject to the jurisdiction of the High court of Kerala.

15.0 TERMINATION OF MOU

15.1 This MoU may be terminated prior to the expiry of the MOU as indicated in para 11 above with six months' notice and with the written consent of the Director, NIELIT CALICUT, Calicut and Head, XXX U. All intellectual property (Designs, Data, Drawings or/and Hardware/Software Developed) will be returned to the respective organization within 15 days of such termination.

15.2 The termination by either party by giving a notice of at least six calendar months is to enable the parties hereto to assess the monetary impact and such other related factors impinging on the interests of the parties. Both parties should honour their respective Academic, Administrative, Technical, and Financial Commitments on the date of receipt of notice of termination.

15.3 NIELIT CALICUT shall have the right to terminate this MOU by giving one month notice if it is satisfied that the programmes being offered at XXX U is not as per the standards as stipulated in the source book and as per the accepted norms in the field of IECT education & training or code of ethics stipulated by NEILIT CALICUT from time to time. The para 10 and 13 shall be valid even after such termination.

16.0 This MoU has been executed in two originals one of these has been retained by NIELIT CALICUT and the other by XXX U

In witness whereof, the parties hereto have signed this MoU on the day, month and year mentioned herein before.

Parties:

For and on behalf of XXX University	For and on behalf of NIELIT CALICUT
Signature	Signature
Name	**Dr. M.P. Pillai**
Designation	Executive Director Calicut Mukkam Road Kerala - 673601
Addresss	India
Witness (Name &Address)	Witnesses (Name & address)

Annexure IIA

1. Post Graduate Diploma in VLSI AND EMBEDDED HARDWARE DESIGN

PREAMBLE

VLSI (Very Large Scale Integration) has emerged as a very significant technology to provide tremendous quantum of processing power and functionality to modern electronic systems. Ubiquitous Computing, Communication and Embedded Systems, based on VLSI are revolutionizing every walks of our daily lives, be it Consumer Electronics, Communication, Computing, Automation, Space Application, Defense and to just about everything. With the advancements in silicon processing technologies for MEMS, NEMS and RF components, many of the formerly external components can now be integrated into a single System-on-Chip which has resulted in a dramatic improvements in performance while achieving reduction in the size, cost and power consumption. Complexity in such systems arises not only from the diversity of the technologies, from sensors and actuators and RF front-ends to base-band DSP software, etc., that must be integrated on-chip comprising of tens of millions of transistors, but also from the fact that such systems must be increasingly built from parts that have been designed separately and using different tools and flows.

Objective of the Course:

- *The PG Diploma in VLSI & Embedded Hardware Design is intended to impart training in designing complex embedded systems using reusable Intellectual Property (IP) Cores as building blocks and employing hierarchical design methods. Emphasis of the teaching curriculum is on design methodology and practical applications. The course contents have been designed keeping in view the emerging trends in needs for skilled manpower. The curriculum has been designed in consultation with industry and academic experts and our strategic partners, to map the skill sets and design methodologies, which is high in demand in VLSI & Embedded Systems industries. Our students have been successfully placed in reputed product companies and we enjoy the trust of many reputed companies, who have entered into strategic alliances with us.*

Outcome of the Course:

This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by Embedded & VLSI markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices.

This uniquely hybrid course makes the successful participants readily employable in multiple roles available in broad spectrum of relevant industries. For people interested in entrepreneurship this would be an excellent launch pad. In addition the course also serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.

Course Structure:

The Course contains 8 modules. The students are required to do a project work in

VLSI and Embedded Hardware Design for a minimum period of 6 weeks to be eligible for issue of PG Diploma in VLSI and Embedded Hardware Design.

Modules

	MODULE NAME	*Duration (Weeks)*
Module 1	Advanced Digital Design	1
Module 2	VHDL Language and Coding for Synthesis	4
Module 3	Verilog Language and Coding for Synthesis	3
Module 4	RTL Verification	3
Module 5	Embedded Controller Based Product Design	3
Module 6	CMOS Logic Design	1
Module 7	FPGA Design Methodology and Prototyping	3
Module 8	Project	6
	Total Duration	24 Weeks (720 hrs)

The student has to submit an internship report to NIELIT Calicut on the completion of course for him/her to be eligible for certificate.

LIST OF MODULES WITH MARKS

	MODULE NAME	*Duration (Weeks)*	*Duration (Hours)*	*Marks*
Module 1	Advanced Digital design	1	30	50
Module 2	VHDL Language and Coding for Synthesis	4	120	200
Module 3	Verilog - Language and Coding for Synthesis	3	90	150
Module 4	RTL Verification	3	90	150
Module 5	Embedded Controller Based Product Design	3	90	150
Module 6	CMOS Logic Design	1	30	50
Module 7	FPGA Design Methodology and Prototyping	3	90	150
Module 8	Project work	6	180	300
	Total Marks	24	720	1200

Hardware /Software Infrastructure Requirements.

Basic Platform:

IBM PCs, One high-end Server
The ratio of the PC/Kits to students should be 1:2
i.e. 2 students would be using 1 PC.

FPGA Trainer Kits:

FPGA Development Boards & Trainer Kits by Altera
FPGA Development Boards & Trainer Kits by Xilinx
PSoC1 and PSoC3 trainer Kits by Cypress Semiconductors

Electronic Instruments: (1: 2)

1. CRO
2. Multimeter (DMM)
3. Power supply,
4. Bread-boards
5. Logic Analyser – 1No

CAD Tools: (1 : 2)

Simulation & Synthesis tools from Mentor Graphics/Cadence/Synopsys
ASIC Design and Verification tools from Synopsys
IC Nanometer tools from Mentor Graphics/ Back end tools from Cadence
Xilinx ISE 12.0 or higher
Altera Quartus II Version11.0or higher
Kiel C for Microcontroller programming
PSoC Designer & PSoC Creator from Cypress Semiconductor
OrCAD/PADS LOGIC for PCB Design

Annexure IIB

2. Post Graduate Diploma in ASIC DESIGN AND VERIFICATION

PREAMBLE

The term ASIC stands for Application Specific Integrated Circuit. It is an integrated circuit (IC) customized for a particular use, rather than intended for general purpose use. Generally an ASIC design will be undertaken for a product that will have a large production run, and the ASIC may contain a very large part of the electronics needed on a single integrated circuit. As feature sizes are shrinking and design tools improved over the years, the complexity in an ASIC has grown to over 100 million gates.

In ASIC Design and Verification process, Verification consumes 50% to 70% of the effort of design cycle and is on the critical path in the design flow of multimillion gate ASICs. Hence verification has become the main bottleneck in the design process. The functional verification bottleneck is an effect of raising the design abstraction level. Majority of ASICs require at least one re-spin, and 71% of re-spins are due to functional bugs. Since ASIC Verification is time consuming, adopting proper verification methodology in ASIC Design flow is extremely important. An ASIC Verification methodology provides the building blocks needed to quickly develop well-constructed and reusable verification components and test environments. FPGA Emulation is another means of verifying complex ASICs, and it helps to capture real time bugs. Studies project that around 5000 highly qualified and trained professionals are required per year.

Objective of the Course:

Education in Engineering Colleges and Universities are severely lagging in meeting VLSI Industry's specific needs, which creates a big gap between the Industry's requirements and the skills of the fresh engineering graduates. Post Graduate Diploma in ***ASIC Design and Verification*** *is structured towards bridging this Industry-Academia gap by providing ASIC/VLSI Industry specific courses with focus on Advanced Technical and Personal Skill development.*

The Course designed in consultation with the ASIC/VLSI industry experts with decades of experience working for various MNCs, builds on the basic concepts in ASIC Design and Verification, and then moves to Advanced ASIC development and Verification Techniques and Methodologies. The course transforms a raw engineering graduate into a capable ASIC Design and Verification professional with both technical and soft skills as required by the industry

Outcome of the Course:

This course is frequently updated in synchronization with the industry to provide the trainees in-depth knowledge and skills required by ASIC Design and Verification markets around the globe. It provides comprehensive understanding about the fundamental principles, methodologies and industry practices. This uniquely hybrid course makes the successful participants readily employable in multiple roles available in relevant industries. For people interested in entrepreneurships this would be an excellent launch pad. In addition the course

also serves as a concrete platform for people involved in application research, consultancy and high end product development in both industry and academia.

Course Structure:

The Course contains eight modules. The students are required to do a project work in ASIC Design and Verification for a minimum period of 6 weeks to be eligible for issue of PG Diploma in ASIC Design and Verification.

Modules

	MODULE NAME	***Duration***
Module 1	Advanced Digital design	1
Module 2	Verilog Language and Coding for Synthesis	3
Module 3	Introduction to ASIC Backend design	1
Module 4	Functional Verification	2
Module 5	Advanced Verification Languages - System Verilog	6
Module 6	DPI and Verification Methodology	1
Module 7	ASIC Prototyping	4
Module 8	Project Work	6
	Total Duration	24 Weeks (720 hrs)

The student has to submit an internship report to NIELIT Calicut on the completion of course for him/her to be eligible for certificate.

LIST OF MODULES WITH MARKS

	MODULE NAME	***Duration (Weeks)***	***Duration (Hours)***	***Marks***
Module 1	Advanced Digital design	1	30	50
Module 2	Verilog Language and Coding for Synthesis	3	90	150
Module 3	Introduction to ASIC Backend design	1	30	50
Module 4	Functional Verification	2	60	100
Module 5	Advanced Verification Languages - System Verilog	6	180	300
Module 6	**DPI and Verification Methodology**	1	30	50
Module 7	ASIC Prototyping	4	120	150
Module 8	**Project Work**	6	180	300
	Total Marks	24	720	1200

Hardware /Software Infrastructure requirements

Basic Platform:

IBM PCs, One high-end Server
The ratio of the PC/Kits to students should be 1:2
i.e. 2 students would be using 1 PC.

FPGA Trainer Kits:

FPGA Development Boards & Trainer Kits by Altera
FPGA Development Boards & Trainer Kits by Xilinx
PSoC1 and PSoC3 trainer Kits by Cypress Semiconductors

CAD Tools:

Simulation & Synthesis tools from Mentor Graphics/Cadence/Synopsys
ASIC Design and Verification tools from Synopsys
IC Nanometer tools from Mentor Graphics/ Back end tools from Cadence
Xilinx ISE 12.0 or higher
Altera Quartus II Version11.0or higher

Annexure IIC

3. Post Graduate Diploma in EMBEDDED REAL-TIME SYSTEMS

PREAMBLE

In today's increasing global market place, successful companies are finding that investments in hardware and software are no longer enough to maintain a competitive edge. Human elements with specialized engineering and design skills have become the essential part of the equation.

Embedded systems monitor and control everything from spacecraft to robots, microwave ovens, car engines, VCRsDVD players, television sets and much more. They control virtually everything that is electronic in our lives. Embedded systems are normally built around Microcontrollers, Digital Signal Processors (DSPs) and FPGAs or SOCs. A lot of trained manpower is required in programming of these tools rather than in hardware design.

Emergence of Embedded operating systems such as Embedded Linux and Android as well as Real-time operating systems helped in developing many exciting applications in embedded products which were unimaginable till recently. Real-time application with big potential in defense sector is another demand area in embedded domain. Mobile communication is one of the fast growing engineering domain of Embedded systems, a lot of emerging technologies are happening in this area such as GSM, GPRS, CDMA, WCDMA, Zigbee, Bluetooth, RFID etc. They make the products smart and are responsible for differentiating the products in the market.

Their huge numbers and new complexity call for a new design approach, one that emphasizes high-level tools and hardware/software tradeoffs, rather than low-level custom programming and logic design. Development of these applications requires sophisticated skills in device driver development, porting etc.

Supplying embedded software to multinational semiconductor and systems companies is likely to be a US$4 billion to $5 billion opportunity for India, according to a study conducted jointly by the Delhi-based National Association of Software and Service Companies (NASSCOM) and New York-based management consulting firm, McKinsey & Co. Revenues from embedded real-time software design are poised for large growth as applicability of embedded systems increases in industries such as Telecom and Datacom, Consumer Electronics, Industrial Automation, Automobiles and Office Automation. A recent Frost & Sullivan study estimated the Indian embedded software market (exclusive of services) at $700 million with an annual growth forecast of 30 per cent. It is estimated that minimum 5000 highly qualified and trained Embedded System professionals are required per year.

To cater to the growing market demand for trained high caliber professionals in Embedded Systems, the Post Graduate Diploma in Embedded Real-time Systems Course is designed. This course covers the fundamentals of Embedded Programming concepts, Real-time operating systems, Porting of OS to Embedded Processors as well as Device Driver development.

Objective of the Course:

To mould fresh electronics & computer science engineers and to retrain working engineers into High Caliber Embedded Real-time Application Designers by enhancing their knowledge and skills in various software design aspects of Embedded Real-time Systems. This course offers a range of topics of immediate relevance to industry and makes the students exactly suitable for industries engaged in Embedded System development. This course is also an excellent preparation for those wishing to engage in application research in this rapidly developing area.

Outcome of the Course:

On completion of the Course, the Participants shall get

- *Expertise in programming language such as C.*
- *Expertise in real-time programming with industry standard RTOS such as VxWorks and RT Linux.*
- *Expertise in Embedded Operating system*
- *Expertise in Device Driver development*
- *Expertise in Porting OS & RTOS to Embedded Processors*
- *Hands on experience in Operating system (Linux) internals*
- *Exposure to Embedded Wireless Application development*

Course Structure:

The PG Diploma in Embedded Real-Time Systems course contains 8 Modules. After completing the first 7 modules, the students have to do a 6 weeks project.

	MODULE NAME	Duration (Weeks)
Module 1	Embedded C and ARM Cortex Microcontrollers	4
Module 2	Embedded Linux	2
Module 3	Embedded RTOS	4
Module 4	Porting On Arm Cortex M3 Microcontrollers	2
Module 5	IOT (Internet of Things) Applications	2
Module 6	Embedded Protocols and Device Drivers	3
Module 7	Seminar and Case Study	1
Module 8	Project Work	6
	Total Duration	24 Weeks (720 hrs)

The student has to submit an internship report to NIELIT Calicut on the completion of course for him/her to be eligible for certificate.

LIST OF MODULES WITH MARKS

	MODULE NAME	Duration (Weeks)	Duration (Hours)	Marks
Module 1	Embedded C and ARM Cortex Microcontrollers	4	120	200
Module 2	Embedded Linux	2	60	100
Module 3	Embedded RTOS	4	120	200

Module 4	Porting On Arm Cortex M3 Microcontrollers	2	60	100
Module 5	IOT (Internet of Things) Applications	2	60	100
Module 6	Embedded Protocols and Device Drivers	3	90	150
Module 7	Seminar and Case Study	1	30	50
Module 8	Project Work	6	180	300
	Total Marks	24	720	1200

Hardware /Software Infrastructure requirements

8-bit 8051 Microcontroller Development System (SBC-51)
32-bit ARM Cortex M3 Microcontroller Development Systems (STM32L Discovery or similar),CAN Development kit, USB Development kit ,SPI Protocol Analyser Kit , I2C Protocol Analyser Kit ,Linux Device Driver Development Kit ,Wireless Modules - Zigbee, Bluetooth, WiFi, GSM, GPS and RFID , Additional components such as Sensors, ARM/ MSP430/ Raspberry Pi/ Beagle/ Arduino boards for project work.
Keil C, WISE-51
gcc Compiler*
Embedded Linux*
VxWorks with ‘x86 BSP
RTLinux with ‘x86
Developer Suite (DS-5) or KEIL MDK - ARM
Chibi OS* or FreeRTOS* or similar
CAN Network Protocol Analyser
USB Protocol Analyser
MATLAB
Glomosim*
* - Open source

Fee Structure and Revenue Sharing.

(No separate fee shall be charged for internship from the students by XXX)

Sl. No.	Course ⟶	VLSI and Embedded H/w Design. ASIC Design and Verification Embedded Real time Systems		
		In corporation Area/Cities	Municipal Areas, Small towns	Panchayat areas, Taluk areas
1	Fees per Candidate(Rs./-)	50,000/-	45,000/-	40,000/-
	Minimum student assured / batch (Nos)	40	30	25

I. The approved institute shall pay 30% of the fee per student collected against each course agreed for conduction at their end

II. Irrespective enrolment, the institute has to pay 30% of fee candidate against the minimum students assured per batch.

III. Fee share mentioned includes Registration / examination & evaluation and Certification.

IV. If the enrolment is more than the minimum assured per batch, proportionate amount at the rate of 30% fee collected from all students is to be paid.

V. Institute may charge less from the students in view of competition / other commitments. However, the NIELIT share will be based on 30% of actual fee indicated against location.

Annexure III - Covering Letter Format

Format for covering letter (To be submitted on the Letter head of the applicant institution)

Ref: _____. Date.

To

The Executive Director
NIELIT Calicut
P B No. 5, NIT Campus P O
Calicut 673 601 Kerala

Subject: EoI for **All India PG Diploma course**

Dear Sir,

1. Having examined the EoI document, we, the undersigned herewith submit our response to your EoI for **All India PG Diploma course**.
2. We have read the provisions of the EoI document and confirm that these are acceptable to us. We further declare that additional conditions, variations, deviations, if any, found in our EoI shall not be given effect to.
3. We would like to declare that we are not involved in any litigation with any state Governments/central Government in India and we are not under a declaration of ineligibility for corrupt or fraudulent practices.
4. We hereby declare that all the information and statements made in this EoI are true and accept that any misrepresentation contained in it may lead to our disqualification.
5. We understand that NIELIT Calicut is not bound to short-list / accept any proposal received in response to this EoI.
6. We understand that Empanelment with NIELIT Calicut does not guarantee that every /any of the applicants shall be invited to bid for, or be awarded a project /assignment.

Our correspondence details / authorized person to deal with regard to this EoI is:

	Information	**Details**
1	Name of the Contact Person	
2	Designation and contact address of the person to whom all references shall be made regarding this EoI	
3	Telephone , FAX number	
4	Mobile number & e mail of the Contact Person	
5	Corporate website URL	

We hereby declare that our proposal submitted in response to this EoI is made in good faith and the information contained is true and correct to the best of our knowledge and belief.

Sincerely,

Signature:
[Authorized person)
Name, title with seal
Encl: Duly filled Application form.

Annexure IV

Application Performa for Expression of Interest for Empanelment of Training Institutes for All India PG Diploma Program		
1	NAME OF THE INSTITUTE	
2	FULL ADDRESS WITH PHONE/FAX/E.MAIL	
3	EOI SUBMITTED FOR	VLSI & Embedded Hardware Design ☐ Embedded Real time Systems ☐ ASIC Design and Verification ☐
4	DATE / YEAR OF ESTABLISHMENT	
5	LEGAL STATUS / REGISTERED UNDER	
6	AFFILIATION	
7	NATURE OF ACTIVITY	
8	COURSES OFFERED AT PRESENT	
9	INFRASTRUCTURE DETAILS (HARDWARE-IT)	
10	INFRASTRUCTURE DETAILS (SOFTWARE)	
11	NO. OF COMPUTER LABORATORIES & DETAILS OF INTERNET CONNECTIVITY	
12	PROXIMITY / NEAR BY TOWNS, HQ, DISTRICT HQ	
13	DETAILS OF ELECTRONICS LABORATORIES	
14	DETAILS OF SIMILAR PROGRAMS CONDUCTED& GOVT. SCHEMES IF ANY	
15	DETAILS OF FACULTIES IN THE AREA OF IT & ELECTRONICS WHO CAN BE SPARED FOR THIS PROGRAM	
16	CONTACT PERSON	
17	DATE FROM WHICH THE PROGRAMS CAN BE LAUNCHED.	
18	IS IT POSSIBLE TO CONDUCT THE TRAINING ON HOLIDAYS & EVENINGS.	
Attach additional sheet, if the space is not sufficient and mark as **Annexure --- (with Sr. No)**		

Attach documentary proof wherever necessary

19. Details of registration fee paid

Amount	Bank	DD No	Date
Rs 1000/-			

20. Signature of Authorized person with Name

20. Declaration

(i) I, _____ son of _____have read and understood the RULES / GUIDELINES for Empanelment of Training Institutes for the implementation of All India PG Diploma Program.

(ii) I certify that I am the competent authority, by virtue of the administrative and financial powers vested in me by_____to furnish the above information and to undertake the above stated commitment on behalf of my /our institution.

(iii) I am aware that in case any information given by me is false or misleading, the Institute would be debarred from the conduction of training programs and / or debarred besides being subjected to any other action that may be deemed fit by NIELIT.

(iv) I agree to abide by the decisions of the NIELIT in respect of my application for permission to Empanel our Institute for the implementation of All India PG Diploma Program

Signature:

Name:

Designation:

Seal of the organization